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(54) **SYSTEM FOR PROCESSING AN ENCRYPTED INSTRUCTION STREAM IN HARDWARE**

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G06F 21/60	(2013.01)
G06F 21/72	(2013.01)
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(52) **U.S. Cl.**

CPC ***G06F 21/602*** (2013.01); ***G06F 21/72*** (2013.01); ***G06F 21/76*** (2013.01)

(58) **Field of Classification Search**

USPC 713/190

See application file for complete search history.

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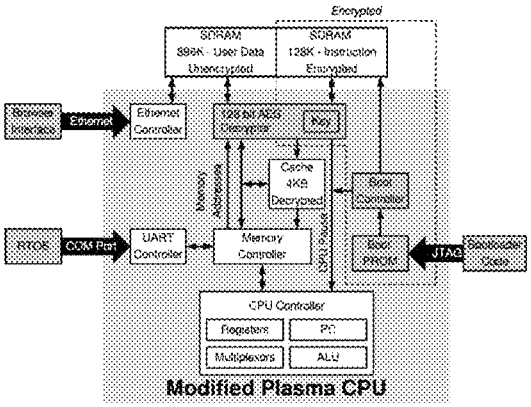
(57) **ABSTRACT**

A system and method of processing an encrypted instruction stream in hardware is disclosed. Main memory stores the encrypted instruction stream and unencrypted data. A central processing unit (CPU) is operatively coupled to the main memory. A decryptor is operatively coupled to the main memory and located within the CPU. The decryptor decrypts the encrypted instruction stream upon receipt of an instruction fetch signal from a CPU core. Unencrypted data is passed through to the CPU core without decryption upon receipt of a data fetch signal.

41 Claims, 5 Drawing Sheets