A Framework for Post-silicon Analog Design Verification and Validation

Vince McKinsey[1], Andrew Elliott[1], Benjamin Hayden[1], Yaser Helal[1],
Adam R. Waite[1], Jon Scholl[1], Jamin McCue[2], Shane Smith[3], and Adam Kimura[1]
[1]Battelle Memorial Institute, Columbus, OH, USA
[2]Air Force Research Lab, Dayton, OH, USA
[3]SenseICs, Columbus, OH, USA

***Abstract*—A post-silicon Analog, Mixed-Signal, and RF (AMS/RF) design verification and validation method was developed called CHARGE (Circuit Hierarchy Analysis, Review, and Graph Evaluation). AMS/RF design verification and validation is important due to the critical role of AMS/RF designs in DoD systems. The CHARGE framework utilizes a Parametric Graph Isomorphism (PGI) algorithm that enables detection and identification of design deviations in AMS/RF circuits. An experiment was devised that tested the CHARGE framework against two AMS/RF designs with deviations in the recovered design and contrasted against golden versions of the same. Experiments in this paper have demonstrated that the CHARGE framework successfully identifies and spatially highlights both structural and parametric deviations in two AMS/RF test articles.**

***Keywords*—verification, validation, hardware assurance, trust, microelectronics, integrated circuits, RF, mixed-signal, analog, GDSII, layout, untrusted foundry**

I. Introduction

Over the last few decades, global economics and market trends within the semiconductor industry have driven modern microelectronics to offshore and untrusted locations for fabrication [1]. With virtually no visibility into the manufacturing supply chain, it is nearly impossible for designers or program offices to know, with any level of confidence, if the integrated circuit (IC) chip has been compromised at a point in the manufacturing process. To address this challenge, post-silicon verification and validation (V&V) techniques have been developed for assuring the manufactured design's equivalence to the trusted golden design [2], [3]. Significant progress has been made over the years with digital design V&V, developing tools that scale to perform equivalence checks between the recovered and golden design across physical layout, function, logic, graph, and timing modalities [4], [5]. These techniques, however, do not map well into the analog domain due to fundamental differences between digital and analog designs. One example of a fundamental difference is the discrete nature of digital versus the continuous nature of analog, which confounds logical and functional checking algorithms. Thus, this limits the number of tools, techniques, and approaches for assuring analog, mixed-signal, and radio frequency (AMS/RF) designs. Microelectronics in modern DoD systems are often complex Systems on a Chip (SoC) that contain sizable percentages of AMS/RF components. Assuring these design modules are equivalent to the golden is critical for a program office to have confidence in the chip's assurance prior to its deployment.

In this paper, we introduce the Circuit Hierarchical Analysis, Review, and Graph Evaluation (CHARGE) framework, a first of-its-kind V&V framework that performs post-silicon V&V on AMS/RF designs. We provide an in-depth review of the CHARGE framework, outline the methodology, and discuss how it aligns and integrates into the larger portfolio of post-silicon V&V techniques. We demonstrate the capability of the CHARGE framework with an experiment that ingests two different AMS/RF designs. The first is a fabricated 14 nm FinFET Configurable Ring Oscillator (CRO) containing design deviations that were fabricated at the foundry. These deviations, however, are not present in the golden GDSII layout. The second is a 14 nm FinFET 4-bit flash Analog-to-Digital Converter (ADC) intended as the mixed-signal component to an RF receiver chain. The deviations elude the traditional functional and logical equivalency checks used in digital V&V, however, the CHARGE framework for AMS/RF V&V is able to identify and flag them for deeper analysis.

II. Limitations of Existing Verification and Validation Approaches

The central issue that differentiates AMS/RF design from digital design is the way analog relates to different mathematical and physical phenomena. This impacts how AMS/RF V&V must be performed, compared to Digital V&V. Digital circuits are restricted to handling boolean algebra through discrete logic. AMS/RF cannot be simplified down to boolean algebra. This can be verified if we consider the Effective Number Of Bits (ENOB) that analog signals can contain due to their continuous nature, which is usually more than one ENOB. Put another way, analog signals can contain more than one bit of information at any given moment, digital signals only ever contain one bit of information. Traditional V&V approaches, such as logical equivalence, solely consider the case when ENOB equals one, which is Boolean Logic. Thus, AMS/RF's continuous nature makes traditional V&V approaches not applicable. AMS/RF circuits can accomplish

certain tasks in far less Power, Performance, and Area (PPA) compared to a digital circuit (e.g., Analog Adder vs Digital Adder or Analog Pulse Width Modulator (PWM) vs Digital PWM). AMS/RF circuits can also perform tasks that digital circuits are incapable of achieving (e.g., Radiating power into space). Consequently, sources of deviation in a design can expand beyond logical failures (e.g., changes in binary logic) to include performance changes (e.g., bandwidth in a filter, gain in amplifiers, slew rate) and physics related changes (e.g., the introduction of negative capacitance, mobility change, or doping change). As such, traditional design verification tools such as Layout vs Schematic (LVS) and Logical Equivalence Check (LEC) do not apply directly to AMS/RF V&V in a post-silicon fabrication context. This limitation of digital design verification tools is illustrated in Figure 1, which also illustrates how the CHARGE framework's new paradigms expand on the existing Digital V&V techniques to include new equivalence check methods that provide coverage over AMS/RF designs. To fully cover the spectrum of functions enabled by AMS/RF systems, a comprehensive solution would compare many electrical effects of the golden design and the recovered design, within a specified tolerance range. For example, solving electromagnetics within materials and surfaces on a large scale with modern computation is currently an active research topic [6]. To that end, we seek computationally feasible methods or techniques that can cover some part of the space covered by AMS/RF circuits.

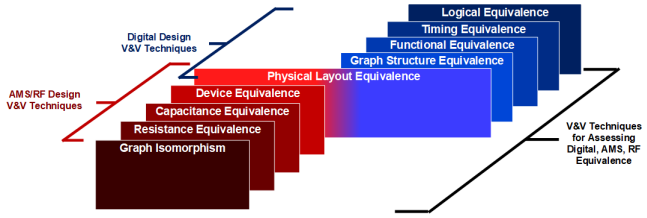


Fig. 1. The CHARGE framework integrates new AMS/RF V&V Techniques into the existing Digital Design V&V Equivalency Checking Techniques from [3], [4] providing a comprehensive post-silicon V&V tool suite for performing assurance on any type of design.

III. AMS/RF V&V Framework

The CHARGE framework introduces a novel approach to post-silicon AMS/RF V&V incorporating concepts across the AMS/RF disciplines. These disciplines usually start at the system specifications, then build up schematics with simulations, and then transition to a parasitic representation that captures first order resistance, capacitance, and inductive effects for greater precision of circuit behavior. Accordingly, the CHARGE framework first analyzes the recovered design schematically for topology and component parameter verification, then validates it at the parasitic level. Schematic level V&V quickly captures deviations in the electrical domain, whereas parasitic level V&V captures deviations in both the physical and electrical domains at the expense of computational complexity. In both cases, the CHARGE framework leverages practices from the existing field of graph theory, by representing extracted circuits as graphs to perform V&V.

Before getting to a graph representation, AMS/RF circuit graph analysis requires Simulation Program with Integrated Circuit Emphasis (SPICE) netlists from both the schematic level and parasitic level. A SPICE netlist is a textual representation of a circuit and includes all necessary components with parameters, component models, and connections. These SPICE netlists are extracted from both the recovered and golden layouts using Cadence Pegasus (or other schematic extraction Electronic Design Automation (EDA) tools) to create SPICE netlists for the schematic. Cadence Quantus (or other parasitic extraction EDA tools) is used to create SPICE netlists that have parasitics included for the layout. Once the proper SPICE netlist is generated, the SPICE netlist is converted into a graph. An example of converting from SPICE to a graph in GraphML format is shown by Figure 2. The conversion is done by taking each net, or electrical device, and creating a node in the graph. Then, edges are connected between graph nodes that represent a connection between a net and a device pin that existed in the SPICE netlist. Additional metadata about position and device parameters are then embedded in the nodes. Once the nodes, edges, and metadata are made, the graph is formed. This graph now enables performing parametric isomorphism checks. Through parametric isomorphism checks, detailed in Section IV, deviations in circuit topology and component parameters can be quickly identified.

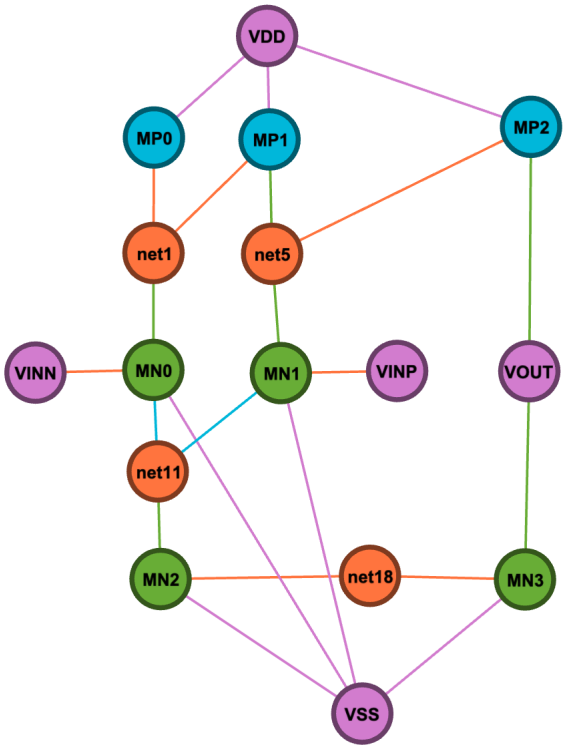
IV. Analysis Methods

The CHARGE framework expands into AMS/RF V&V by introducing new paradigms into the V&V space that traditional V&V approaches can't handle when dealing with AMS/RF designs. This new approach, called Parametric Graph Isomorphism (PGI), is applied on circuit graphs that are generated from SPICE netlist files. This graph then undergoes partitioning to reduce the complexity of the search space. The resulting graphs are then digested by PGI to perform the comparison and equivalence checks to find deviations in the recovered design. The comparison and equivalence checks expand beyond pure graph isomorphism by additionally being able to compare the metadata of the nodes. This means the tools can be used to compare component values (such as resistance or capacitance) or any other data that is included in the metadata (such as location of the devices). The process for this analysis is shown in Figure 3, wherein two layouts, one for the golden design and one for the recovered design, are ingested into a parasitic extraction (PEX) tool to produce a SPICE netlist.

The concept of PGI is a derivative of Graph Theory's isomorphism [7], wherein we compare the graph structure between the golden graph and the recovered graph. In PGI, two nodes, one in the golden graph and one in the recovered graph, are considered "matches" if the nodes have the same connectivity and metadata within a specified tolerance. The specified tolerance is to account for process variations and imaging errors, which allows PGI to show gradients of change

```
.SUBCKT opamp VDD VINN VINP VOUT VSS
MP2 VOUT net5 VDD VDD pfet m=1 l=14n nf=1 nfin=2 fpitch=48n cpp=78n ngcon=1
+ p_la=0 plorient=0 analog=-1.0
MP1 net5 net1 VDD VDD pfet m=1 l=14n nf=1 nfin=2 fpitch=48n cpp=78n ngcon=1
+ p_la=0 plorient=0 analog=-1.0
MP0 net1 net1 VDD VDD pfet m=1 l=14n nf=1 nfin=2 fpitch=48n cpp=78n ngcon=1
+ p_la=0 plorient=0 analog=-1.0
MN3 VOUT net18 VSS VSS nfet m=1 l=14n nf=1 nfin=2 fpitch=48n cpp=78n ngcon=1
+ p_la=0 plorient=0 analog=-1.0
MN2 net11 net18 VSS VSS nfet m=1 l=14n nf=1 nfin=2 fpitch=48n cpp=78n ngcon=1
+ p_la=0 plorient=0 analog=-1.0
MN1 net5 VINP net11 VSS nfet m=1 l=14n nf=1 nfin=2 fpitch=48n cpp=78n ngcon=1
+ p_la=0 plorient=0 analog=-1.0
MN0 net1 VINN net11 VSS nfet m=1 l=14n nf=1 nfin=2 fpitch=48n cpp=78n ngcon=1
+ p_la=0 plorient=0 analog=-1.0
.ENDS
```

(a) The SPICE netlist extracted from a generic amplifier made in 14 nm FinFet technology.



(b) The equivalent graph of the previous SPICE netlist.

Fig. 2. An example of an amplifier SPICE netlist (a) being converted to a graph (b). The edges of the node lead to the voltage nodes (orange) of the device in SPICE. Data about the device given on the SPICE line (such as number of fingers, Length, or Width) is stored in the metadata of the node. Note that the voltage nodes themselves are also nodes in the graph. Those voltage nodes then lead to other nodes via edges.

on component and parasitic values. This enables highlighting regions of interest for highly deviated components. However, these tolerance values must be chosen carefully. Too large of a tolerance range could result in failure to identify a deviation (Type II), but setting the threshold too tightly may result in large amounts of false positives (Type I) due to small process variations that would not be expected to cause deviated behavior. An example of the various deviations that can be captured by this tool is illustrated in Figure 4, wherein we see not just missing nodes, but nodes that have various design parameters altered. PGI effectively enables equivalence checking of electrical, physical, and other relevant parameters in not only designed devices of post-silicon layouts but also parasitic elements.

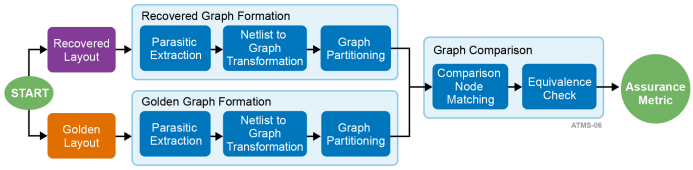


Fig. 3. Overview flow diagram showing the general flow of the analysis. Two layouts, one for the golden design and one for the recovered design, are ingested into a PEX tool to produce a SPICE netlist. That SPICE netlist is transformed into GraphML and undergoes graph partitioning to reduce the complexity of the search space. The resulting graphs are then digested by PGI to perform the final comparison and equivalence checks to find deviations in the recovered.

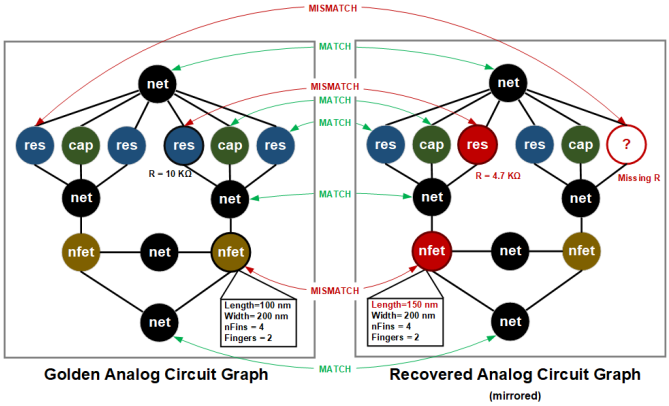


Fig. 4. Example golden vs. recovered parametric graph isomorphism, showing a mismatch on one of the resistors, a match on two of the nets, and a mismatch on a parameter in one of the NFET devices. Mismatches can also be found in capacitance values, voltage nodes, etc.

V. Experimental Setup

In order to demonstrate the CHARGE framework's ability to ingest and parse an AMS/RF design, compare it to a trusted golden reference version, and identify deviations, an experiment was performed on two AMS/RF designs as test cases for validating our post-silicon AMS/RF assurance approach. These chosen designs were a CRO from the Headache chip and a 4-bit flash ADC from the Insomnia chip.

A. 14 nm FinFET Headache Configurable Ring Oscillator

The first design, dubbed the Headache chip, was designed and fabricated in a 14 nm FinFET technology and contained a variety of AMS/RF circuits. Our work focused on a ring oscillator design, which serves as an entropy source for a True Random Number Generator circuit that generates cryptographic keys. Headache version A represents the golden reference layout sent to the foundry. Headache B is a cloned version of Headache A that contains small, stealthy variations in the AMS/RF circuitry that impact the performance of the ring oscillator circuit. The Headache B chip is representative

of the threat case where a modification was made at some point in the manufacturing supply chain. These changes elude the traditional digital post-silicon V&V techniques.

B. 14 nm FinFET Insomnia Analog-to-Digital Converter

The second design considered, called the Insomnia chip, implements a 14 nm RF receiver chain, consisting of a Low Noise Amplifier (LNA), Mixer, Lowpass Filter (LPF), and a 4-bit flash ADC. The Insomnia chip has two versions of this RF chain implemented on-chip. The first version is a "golden" reference chain, which serves as the "ground truth" for the entire chain. The other version is a "deviated" chain, which represents a scenario where a modification was made at some point in the manufacturing supply chain. Each block of the chain (the LNA, the mixer, the LPF, and the ADC) had deviations introduced that were analog in nature. This work focuses on analyzing the variant ADC block of the Insomnia chip.

C. Setup Summary

The Headache chip's CRO deviation replaces several fill cells, which is a change that is detectable using existing analysis techniques [3], [4], allowing us to validate our methods against a known result. Insomnia's flash ADC deviation is purely resistive in nature, made by increasing the length of metal lines to increase resistance. This deviation would elude traditional logic and function V&V approaches used for digital circuits.

Each GDSII file was loaded into Cadence Quantus in order to perform a PEX. In all cases, capacitive and resistive extraction was performed using identical settings. These extracted SPICE netlists were then converted into graphs and the graphs were processed using PGI to detect and identify anomalies in the deviated layouts. The question we ask is: *can the CHARGE framework capture those modifications that elude other established V&V techniques, enabling AMS/RF V&V?*

VI. Experimental Results and Analysis

A. 14 nm FinFET Headache Configurable Ring Oscillator

We first recovered the full circuit design files by applying sample delayering, imaging, and feature extraction techniques across the entire 14 nm FinFET design stack-up of Headache B [8], [9]. We then extracted the as-fabricated layout from Headache B and ingested it and the golden Headache A layout into the CHARGE framework for comparison, according to the flow diagram shown in Figure 3. Once analyzed, the framework identified the deviations within the AMS/RF circuit graphs and highlighted the areas requiring deeper inspection. Using our PGI approach, we detected and determined that the changes made to Headache B were decoupling capacitor fill cells being switched out for normal fill cells with no capacitors. We found 492 deviated devices due to the missing via connections in the ring oscillator. Figure 5 shows the region of interest and the extracted cells of the ring oscillator as well as highlighted transistors impacted by the modifications.

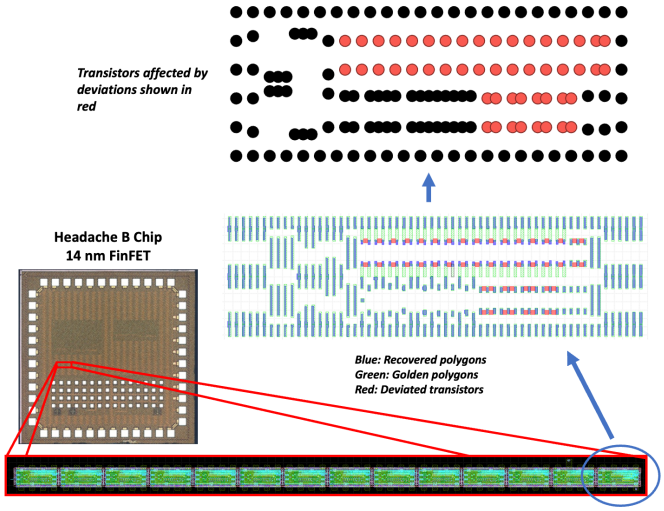


Fig. 5. Headache B was ingested into the CHARGE framework and analyzed against Headache A for deviations in the AMS/RF circuitry. One stage of the ring oscillator is shown with the affected transistors in red and non-affected transistors in black due to the introduced deviations.

B. 14 nm FinFET Insomnia Analog-to-Digital Converter

Next, we took a single variant of the 4-bit ADC from the Insomnia chip, seen in Figure 6, and applied PGI against the golden 4-bit ADC from the same chip. The PGI algorithm then produced a graph with marked nodes which represent devices that had parameters out of tolerance as seen in Figure 7. Using the positions of the devices, the out-of-tolerance devices can be located in the layout for further inspection.

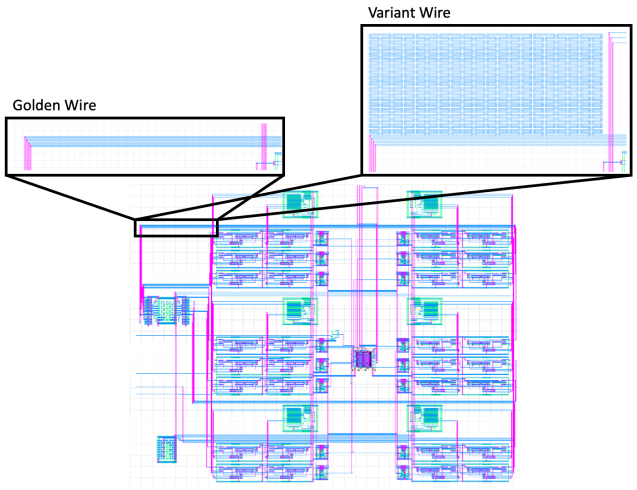


Fig. 6. ADC Variant layout showing both the golden and variant versions of the affected wire.

C. Experimental Summary

These two experiments show that PGI is an effective method for determining AMS/RF deviations in designs. Using PGI,

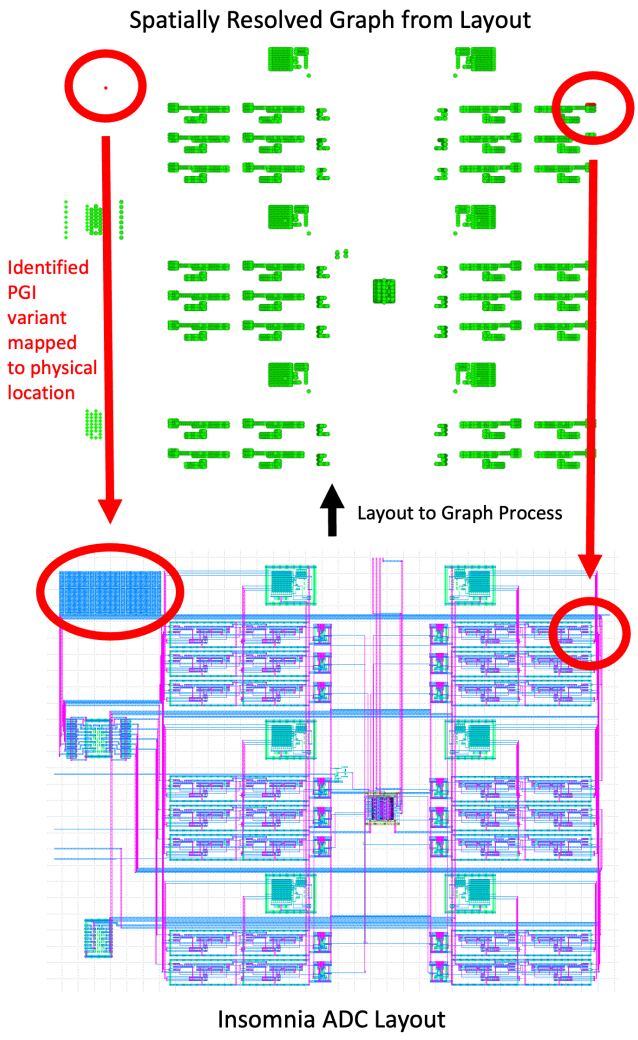


Fig. 7. ADC Variant layout (shown at the bottom) contrasted with the PGI generated graph (shown at the top) showed the approximate location of the variant that have been marked due to parameters being out of tolerance. The left most circle is the actual wire that the variant changed. The right most circle is the effect the variant had on the connectivity of the layout.

the CRO in Headache completed in 1.47 minutes, which had a layout area of 560 μm^2. The ADC in Insomnia completed in 45.31 minutes, which had a layout area of 21,970 μm^2. The PGI tool runtime and design size table is shown below in Table I along with additional information about graph sizes and layout area.

VII. Discussion

Experiments have demonstrated that the CHARGE framework successfully identifies and spatially highlights both structural and parametric deviations in two AMS/RF test articles. The introduction of PGI into the problem of post-silicon AMS/RF V&V represents a powerful capability by being able to detect and identify deviations that are present due to topological and parasitic effects in a design, in addition to connectivity and component-value checks present in a standard LVS comparison. Besides the example of resistance shown in this work, PGI can detect and identify deviations in other electrical properties such as capacitance, or any other numerical property, in the same way. By visually highlighting the deviated area for the user and reporting the type of deviation encountered, the framework can be used by a V&V team to pinpoint the deviation for further analysis.

After PGI approximately located the deviations, a circuit designer with AMS/RF experience analyzed the function of the deviations that were found. For the CRO, it was concluded that certain FILL cells were replaced with changed FILL cells that presented different capacitance. The changed capacitance would change the CRO's typical oscillation frequency, which was subsequently validated using Cadence Spectre. For the ADC, it was determined was that additional resistance was being added into the feed wire from the reference circuit to the ADC's comparators. The additional resistance would impact the kickback from the ADC's comparators in the comparator ladder, which was subsequently validated using Cadence Spectre.

A factor limiting the effectiveness of the CHARGE framework is the scaling of the approach. While the graph isomorphism problem is of NP-intermediate complexity [10], PGI reduces this complexity by further constraining node matches based on parametric values. Runtime can be reduced by increasing the minimum parasitic thresholds during PEX, at the cost of decreased resolution of the parasitic graph. In practice, default PEX settings for the PDK used to design the test articles resulted in graphs of a size that were not tractable for our current implementation. By reducing minimum PEX values, we extracted graphs that PGI checks were able to process in under an hour on our test articles running on a standard workstation.

While the CHARGE framework was developed with AMS/RF V&V in mind, the methodology described here can be applied to digital circuits as well. Deviations in a digital circuit that arise due to complex analog behaviors are not detectable when modeling the circuit logically. By considering a digital design as an analog system, the CHARGE framework can be applied to digital circuits to identify deviations that exist due to these analog effects, thereby providing additional modalities of deviation detection and identification. Once deviations are detected in a digital design, information provided by the CHARGE framework about the location and nature of the deviations can be utilized to further investigate the logical effect that the deviations may cause. Due to the complexity and density of modern digital circuits, further optimizations may be necessary to ensure analysis can be completed in a timely fashion.

VIII. Conclusions

This work extends existing post-silicon V&V science beyond the digital domain and into the AMS/RF domain. Here, we provided a newly developed proof-of-concept framework designed to detect and identify deviations in AMS/RF circuits after fabrication. For this demonstration, a real-world

TABLE I
PGI TOOL RUNTIME AND DESIGN SIZE

Device	Area (μm^2)	# of Devices	# of Nodes	# of Edges	Time (mins)
CRO Variant	∼560	2160	4744	8640	1.47
CRO Golden		2160	3883	8640	
ADC Variant	∼21970	9440	12022	36920	45.31
ADC Golden		9439	12020	36918	

Note: "# of Devices" is the number of resistors + number of capacitors + number of transistors

fabricated chip that contained modifications in the AMS/RF circuitry, in addition to a newly developed AMS/RF chip currently being fabricated, were selected for V&V. We applied our physical design decomposition and design file extraction approach to recover the as-fabricated layout and ingested it with the golden layout into the CHARGE framework for detection and identification of unknown design deviations. Finally, we successfully identified and located all the deviations, thus demonstrating its potential to address the challenge of ensuring the integrity of AMS/RF components on manufactured chips. There are several avenues that could be explored for future work. Research for techniques and methods to capture radiative effects, such as those experienced by antenna and RF circuits in general, is ongoing. Future research should also seek to cover material effects.

ACKNOWLEDGEMENT

Funding Acknowledgement: This research was sponsored by the Air Force Research Lab as part of the OUSD Trusted and Assured Microelectronics Program.

REFERENCES

[1] M. Tehranipoor and F. Koushanfar, "A survey of hardware trojan taxonomy and detection," *IEEE Design & Test of Computers*, vol. 27, no. 1, pp. 10–25, 2010.

[2] A. R. Waite, J. H. Scholl, J. Baur, A. Kimura, M. Strizich, and G. D. Via, "IC decomposition and imaging metrics to optimize design file recovery for verification and validation," in *ISTFA 2020: Papers Accepted for the Planned 46th International Symposium for Testing and Failure Analysis*. ASM International, Dec. 2020.

[3] A. Kimura, J. Scholl, J. Schaffranek, M. Sutter, A. Elliott, M. Strizich, and G. D. Via, "A decomposition workflow for integrated circuit verification and validation," *J. Hardw. Syst. Secur.*, vol. 4, no. 1, pp. 34–43, Mar. 2020.

[4] K. Liszewski, T. Mcdonley, J. Delozier, A. Elliott, D. Jones, M. Sutter, and A. Kimura, "Netlist decompilation workflow for recovered design verification, validation, and assurance," *Cryptology ePrint Archive*, pp. 1–8, 2021.

[5] A. Waite, J. Kelley, J. Scholl, Y. Patel, J. Baur, J. Schaffranek, V. Mckinsey, G. D. Via, and A. Kimura, "Verification and validation of a 45 nm node device utilizing a novel homeomorphic error checking tool for intelligent feature extraction," in *Government Microcircuit Applications & Critical Technology (GOMAC Tech) Conference*, 2021.

[6] D. P. Zoric, D. I. Olcan, and B. M. Kolundzija, "Solving electrically large em problems by using out-of-core solver accelerated with multiple graphical processing units," in *2011 IEEE International Symposium on Antennas and Propagation (APSURSI)*, 2011, pp. 1–4.

[7] A. Bondy and U. Murty, *Graph Theory*, 1st ed. Springer London, 2008.

[8] A. R. Waite, Y. Patel, J. J. Kelley, J. H. Scholl, J. Baur, A. Kimura, E. D. Udelhoven, G. D. Via, R. Ott, and D. L. Brooks, "Preparation, imaging, and design extraction of the front-end-of-line and middle-of-line in a 14 nm node finfet device," in *2021 IEEE Physical Assurance and Inspection of Electronics (PAINE)*, 2021, pp. 1–6.

[9] A. Kimura, A. Waite, J. Scholl, J. Kelley, J. Schaffranek, E. Haines, T. McDonley, K. Liszewski, Y. Patel, J. Baur, and et al., "Applied microelectronics assurance verification and validation for unknown variant identification and analysis in a fabricated 14 nm finfet design," *Government Microcircuit Applications & Critical Technology Conference (GOMAC Tech)*, Mar 2022.

[10] U. Schöning, "Graph isomorphism is in the low hierarchy," *Journal of Computer and System Sciences*, vol. 37, no. 3, pp. 312–323, 1988. [Online]. Available: https://www.sciencedirect.com/science/article/pii/0022000088900104