

Electromagnetic Transient Modeling of Large Data Centers for Grid-Level Studies

Beta Release

August 2026

Brett A. Ross
Sameer Nekkhalapu
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U.S. DEPARTMENT
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Pacific Northwest National Laboratory
Richland, Washington 99354

Abstract

The magnitude and complexity of electricity usage patterns from large data centers are having significant impacts on the operation and dynamics of the power grid; grid operators and planners require a range of specialized data center models to properly evaluate these impacts and specify technical solutions as needed. Towards addressing this need, Pacific Northwest National Laboratory (PNNL) has developed a library of electromagnetic transient (EMT) models for grid-level studies of data centers called the data center model library (DML). This report describes how the DML was created and how it may properly be used.

This report details the DML's beta release, completed in July 2026. This is a revision and expansion of the alpha release, which was made available in January 2026 [1].

The models present in the DML are generic models; subject matter expertise and additional technical data are needed to modify these models before they can represent any real data center. However, they will significantly reduce the level of effort required to develop site-specific models and can serve as a common starting point to guide industry towards a more refined consensus.

Most of the models within DML are dedicated to representing the power electronics interfaces commonly used in modern data centers, such as double-conversion uninterruptible power supplies and single-phase power factor correction converters. These models are intended for use in grid-level studies and are a simplified aggregation of many small components. That said, background material on the physical and electrical design of large data centers is provided as companion material so that users can be aware of many of the details which have been omitted or streamlined as a matter of practical necessity. Additionally, guidance on the application of EMT analysis for data center interconnection studies is provided, which aids users in identifying when the DML is necessary and what sort of additional model development may be necessary for conducting real-world studies.

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have sent us many kind words, useful feedback, and helpful suggestions since the library was first released in early 2026. Many of the model improvements and additions were directly inspired by this input.

Acronyms and Abbreviations

AI	Artificial intelligence
AVM	Average-value model
ASIC	Application-specific integrated circuit
BoP	Balance of plant
CPU	Central processing unit
CRAH	Compute-rack air handler
DC	Direct current
DML	Data center modeling library
EMT	Electromagnetic transient
ESIG	Energy Systems Integration Group
ESS	Energy storage system
FACTS	Flexible AC transmission systems
GFL	Grid following
GFM	Grid forming
GPU	Graphics processing unit
GSU	Generator step-up
HV	High voltage
IBR	Inverter-based resource
IT	Information technology
ITE	Information technology equipment
LLTF	Large loads task force
LV	Low voltage
LVDC	Low voltage direct current
LVRT	Low voltage ride through
NERC	North American Electric Reliability Corporation
NPC	Neutral-point clamped
MMC	Multi-level modular converter
MV	Medium voltage
OEM	Original equipment manufacturer
PCC	Point of common coupling
PFC	Power factor correction
PH	Phase
PLL	Phase-locked loop
PWM	Pulse-width modulation
SSCI	Subsynchronous control interaction
SSTI	Subsynchronous torsional interaction
SST	Solid-state transformer
SWM	Switching model
UPS	Uninterruptible power supply
VAC	Virtual admittance control
VSC	Voltage-source converter

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1.0 Introduction

In recent years, the energy consumption patterns of data centers have grown considerably in magnitude and complexity, resulting in substantial consequences for the operation of the power grid at large. Grid planners and operators need models in order to proactively evaluate the effects of interconnecting data centers on the grid. These evaluations can be used to determine the performance restrictions and technical solutions necessary for reliable integration of data centers.

Many studies must be performed to evaluate grid impacts from a large data center, and different kinds of studies require different kinds of models. Of the many kinds of models needed, this work's focus is on electromagnetic transient (EMT) modeling of data centers. EMT modeling is one of the highest-fidelity forms of modeling used in power system analysis and significant expertise and technical data is required to construct a reasonable EMT model. The purpose of this work is to accelerate industry's ability to develop suitable EMT models of data centers.

Pacific Northwest National Laboratory (PNNL) has developed a library of generic EMT models, referred to as the data center modeling library (DML), using the power systems computer-aided design (PSCAD), a tool widely used in industry to simulate electromagnetic transients in power systems. The DML has been made freely available and most of this report is dedicated to explaining how DML was developed and how it may be used productively. The models in DML are intended for studying the aggregate effects of data center components on the power grid; they are of limited use for studying design problems or disturbances within the data center itself.

This report details the DML's beta release, completed in July 2026. This is a revision and expansion of the alpha release, which was made available in January 2026 [1].

The DML is not a realistic representation of any one data center, nor is it intended to be. Rather, it is a reasonable starting point for the development of site-specific models for use in grid-level studies. Site-specific models must be developed using subject-matter expertise and site-specific technical data. A wide range of common data center components have been implemented along with organizational features intended to reduce the additional labor needed to make the models site specific. Lessons learned, typical design practices, and opportunities for simplification have been documented to aid engineers in managing the potentially impractical level of complexity involved in EMT model development.

This report's contents are organized as follows. Section 2.0 describes the design of power systems used within data centers and presents six aggregated site models which can be used to represent most modern or near-future data centers. Section 4.0 discusses practices for EMT modeling of data centers, explaining the situations in which it is beneficial to undertake the time-consuming process of performing an EMT study and the kinds of risks and challenges such a study can articulate. Section 5.0 describes in detail how the different components of data center power systems can be represented in an EMT model and how this relates to the components provided in DML. Section 5.4 describes the power system models included in DML and documents their functionality. Section 6.7.4 documents the functionality of the individual component models included in DML.

2.0 Changes from Alpha Release

This section documents changes made to the DML from the previous alpha release.

2.1 Component Model Improvements

- Improvements to DC-DC converter models (`DC_bi_avm`, `DC_bi_swm`)
 - **New feature:** Dynamic control mode selection. If desired, an external control signal can now be used to dynamically select the DC-DC converter control mode during simulation. Alternatively, the control mode may be fixed to either active power regulation or DC voltage regulation.
 - **Fix/Improvement:** Reworked dynamic DC voltage regulation controls. Originally, two PI controllers and limits were used to allow simultaneous active power and DC link voltage regulation. This simplified approach provided stable and qualitatively correct behavior but also resulted in unrealistic active/reactive power transients and is impractical in reality. Now, a single PI control with dynamic signal source and gains is used and, in UPS applications, controlled by the undervoltage ride-through logic of the rectifier model (`inv_gfl_avm`). Additionally, a feedforward proportional DC voltage regulator is added in parallel to mitigate large DC voltage fluctuations during control mode transitions.
- Improvements to inverter model with grid-following control (`inv_gfl_avm`)
 - **New feature:** Voltage threshold to exit momentary cessation. Previously, the same voltage threshold setting was used to both enter and exit momentary cessation. Now the two thresholds are separate settings.
 - **New feature:** Output signals for control status for features such as voltage sag detection and momentary cessation.
 - **Fix/Improvement:** The handling of current limits during and immediately after momentary cessation has been significantly reworked to eliminate unrealistic active and reactive power transients. Active and reactive current are now handled differently from one another with respect to limiting, reset, and rate limiting during momentary cessation (MC) and post-MC reconnection. The freeze, reset, and unfreeze process for the active current now provides a smoother response during changes in inverter and battery converter control modes. The reactive current control now remains active during reconnection and ensures unity power factor operation.
- Improvements to PFC converter models (`pfc_avm` and `pfc_swm`):
 - **Bug fix:** `pfc_swm` had an error in the scaling of the AC current measurement that was causing AC current overcurrent to trip at incorrect thresholds.
 - **New feature:** AC current limiting. Previously, DC voltage regulator output was limited to avoid unrealistic overcurrent conditions which could cause numerical instability. However, this approach excessively reduced power supply current

consumption during voltage sags, resulting in behavior closer to constant impedance rather than the expected constant power operation. Now, this output limit has been increased and a current-scaling based current limiter is used, allowing the user to tune the model to a particular power supply's fault response.

- **New feature:** Variable DC-side loading. Previously, built-in DC-side load was automatically set to 1 pu. Now, this is an input parameter which supports variable signals if the user wishes to simulate a varying load profile.
- **New feature:** Rate-limited reconnection after entering momentary cessation, similar to that provided in `gfl_ibr` and used in practical rack-level power supplies to ensure a graceful transition to on-site backup generation.
- **New feature:** External outputs for control bits (SAG, MC, WALKIN) for use with DC-DC converter models. These are used to switch the newly-improved DC-DC converter control into DC voltage regulation mode when the PFC converter is tripped offline or otherwise limited.
- Improvements to existing diode rectifier models (`rect_3x_full_wave`, `rect_3x_full_wave_c`, `rect_six_pulse`)
 - Added support for variable loading. Prior models assumed that the rectifiers were operating at nominal load, whereas most diode rectifier loads (e.g., motor drives) run at part or low load the vast majority of the time. This strongly affects the rectifier's response to AC voltage sags.

2.2 Power System Model Improvements

- Improvements to DML_PFC_Demo:
 - Minor changes to accommodate improvements to `pfc_swm` and `pfc_avm`, components for testing presence of DC-side battery converter have been removed as this implementation is now more complex and robust—see `DML_DC3_Distributed` for an example implementation.
- Improvements to the Simple Data Center model (`DML_DC1_Simple`):
 - Added passive harmonic filters to bring site within compliance of IEEE 519 limits for a large HV-connected facility.
- Improvements to Centralized UPS Data Center model (`DML_DC2_Central_UPS`):
 - Added digital logic to UPS model to take advantage of new control implementation for battery converter (`DC_bi_avm`).
 - UPS control gains and parameters have been re-tuned to account for changes in the design of the `inv_gfl_avm` and `DC_bi_avm` components.
 - Reconfigured UPS inverter to make use of the new AC voltage regulator added to `gfm_droop`.

- Added passive harmonic filters to bring site within compliance of IEEE 519 limits for a large HV-connected facility.
- Improvements to Distributed UPS Data Center model (DML_DC3_Distributed)
 - Added passive harmonic filters to bring site within compliance of IEEE 519 limits for a large HV-connected facility.
 - Adjusted connectivity and parameters of PFC converters and battery converters to account for changes in the design of DC_bi_avm and pfc_avm.
 - Component sizing now accounts for the fact that cooling components operate only at part load.

2.3 New Component Models

- New models for representing variable frequency drives (vfd_avm, vfd_swm, vfd_avm_1PH, vfd_swm_1PH) which commonly provide building-level cooling for data centers.
- New model for representing generators driven by reciprocating internal combustion engines (gen_recip).
- New model for automated synchronization of synchronous generators via synchronism check and speed control (gen_sync).

2.4 New Power System Models

- New example case, DML_Gen_Demo, which demonstrates use of the new reciprocating engine and autosynchronizer models.
- New example case, DML_Drive_Demo, which demonstrates use of the new variable frequency drive models.
- New example case, DML_PERC1_Demo, which illustrates a comparison of the double-conversion UPS model with the PERC1 phasor model as implemented in PSSE and Powerworld.
- New data center model, DML_DC4_Mixed, for representing data center campuses which may have different blocks each used for differing customer bases.

3.0 Data center Power Systems

The purpose of this section is to provide a succinct overview of those aspects of data center power systems that are most relevant for grid level dynamic studies. This highlights the major components needing representation in various studies and outlines current and near-future archetypes for data center design.

3.1 Power Electronics Topologies

Most grid-level EMT studies involving data centers employ relatively simple representations of the site distribution systems, with most of the model fidelity being concentrated on the power electronics that support information technology equipment (ITE). The power electronic architectures for most data centers fit into one of six designs—these are described below, and single-line diagrams of the proposed aggregated EMT models are provided. The first three designs are in use today and case files for them are included in DML. The later designs range from near future (e.g., within 2 years) to futuristic (e.g., within 10 years) and the alpha release of DML does not include all of the component models required to represent these systems. A more detailed discussion of the reasoning behind selecting the specific components shown within the single-line diagrams may be found in Section 5.0.

Design 1: Simple

The simple data center design is primarily associated with cryptomining operations and seldom used for other applications (Figure 1). Compared to most other data centers, reliability is less critical and the costs associated with the electric plant are more influential on the site's economic viability. AC/DC conversion at the rack level is done at 240 V and diode-based power factor correction (PFC) converters are used. No uninterruptible power supply (UPS) or on-site backup generation is present.

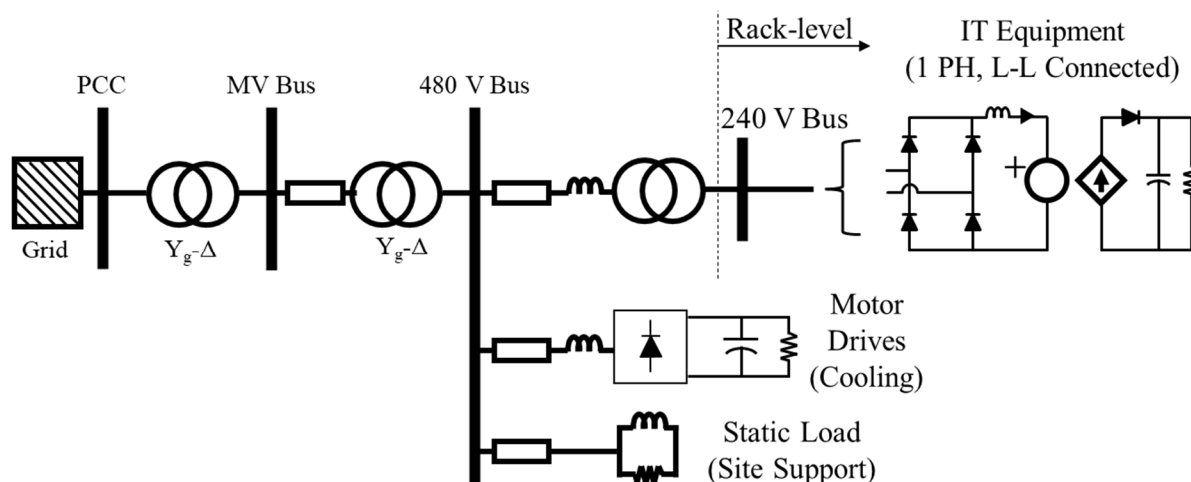


Figure 1: Single Line Diagram of Simple Data Center Design.

Design 2: Centralized UPS

The centralized UPS design is likely the most common for many data centers currently in operation (Figure 2). ITE is located behind large (~1 MVA each) three-phase UPS to protect it

from grid disturbances and ensure continuity of service in the event that the data center must disconnect from the grid and start up local backup generators. While not considered in grid-level studies, high voltage (HV) and medium voltage (MV) systems are equipped with numerous alternate feeds and automatic transfer schemes. Data centers of this design are often designed for concurrent maintainability and achieve Tier 3 reliability as defined by the Uptime Institute [2]. On-site generation is provided and consists of either distributed diesel engines or large steam or natural gas turbines. Traditionally, these are never paralleled with the grid and are only used after the data center has disconnected from the grid following a disturbance. The UPS batteries are used to supply the load in the interim period. However, a recent trend has been for on-site generation to become part of the grid's generation pool and to provide occasional support in order to manage grid-level generation shortages or transmission congestion.

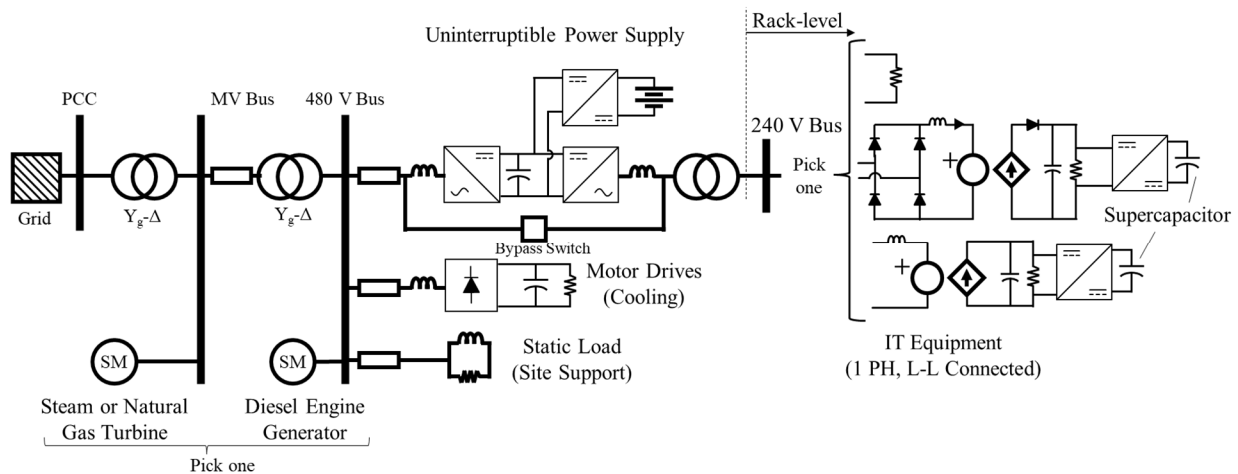


Figure 2: Single Line Diagram for Centralized UPS Data Center Design.

A single UPS serves a number of IT racks, with modern per-rack power demands typically in the tens of kilowatts for traditional applications and over 100 kilowatts for high-performance computing (i.e., AI training) applications. The rack level power supplies may be modeled as a simple resistive load (potentially with a time-varying demand) unless the UPS is operated with the bypass switch closed. Single phase power supplies are represented in Figure 2 using the average-value model (AVM) for both unidirectional (diodes shown) and bidirectional (no diodes shown) models for a voltage-source converter to illustrate that either may be used. More detail on this is given in Section 5.1.

There are many variations on the centralized UPS design on a site-to-site basis. Some or all of the cooling load at a site may be behind UPS as well—this is increasingly common in artificial intelligence (AI) applications as high heat densities and hardware costs make the risks associated with temporary cooling interruptions more significant. Some of the motor load may consist of line-connected induction motors rather than motor drives.

Supercapacitors at the rack level are newly come to market [3] and are present at few sites at the time of writing. Their primary application is smoothing of rapid changes in compute load (e.g., due to hyperscale AI training) in order to reduce both site- and grid-level disruptions. However, they may also come to be utilized to improve the site's ride-through capabilities as well.

7

Increased power density needs of AI platforms are the primary motivation for original equipment manufacturers (OEMs) and data center developers to expend significant capital on developing DC distribution systems—present-day graphics processing unit (GPU) racks attain 120 kW, and prototypes up to 1 MW have been developed and planned for 2027 [11] [8]. Training larger and more sophisticated AI models requires more compute resources, and a high degree of low-latency connectivity between individual processors is required for good performance during training. The latency and bandwidth constraints this introduces make it prohibitive to continue spreading compute resources over a wider area, and the result is a strong demand for the high power densities which only DC power systems can provide.



Design 4: Low-Voltage DC Distribution

The low voltage DC (LVDC)¹ distribution design is a central R&D focus for many OEMs [7] [15] and is in the prototype stage (Figure 4). It is also seen as somewhat of a stepping stone to the later two architectures, which require additional R&D and field experience with operating DC distribution systems. From an aggregated perspective, this design may be viewed as a variation of the centralized UPS design wherein the output inverter is absent and the DC link voltage (either 400 V or 800 V, depending on the vendor [11] [16]) is distributed directly to individual racks of IT equipment. The design of the 480 V rectifiers will likely be similar to those employed in double-conversion UPS today. The rack-level power supplies are no longer single-phase AC/DC converters but rather DC/DC converters which step the 800/400 VDC down to 50 VDC for ITE to use.

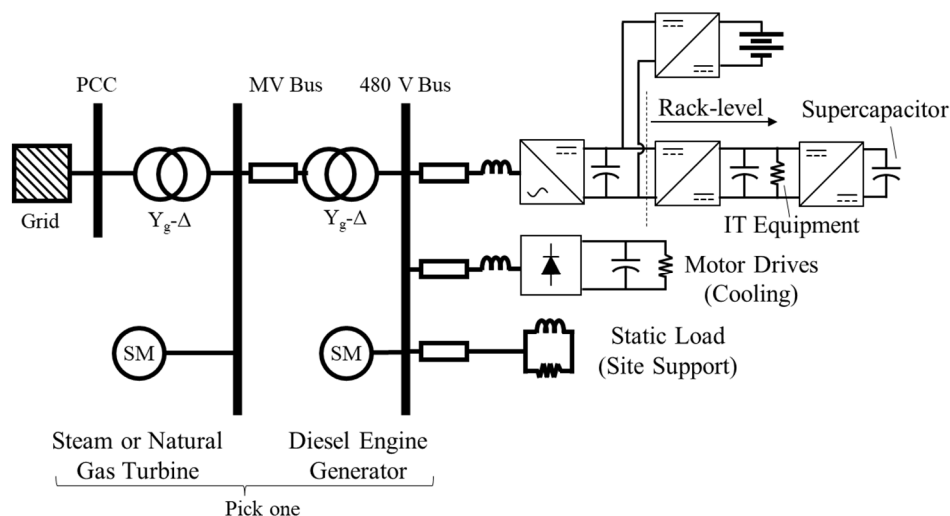


Figure 4: Single Line Diagram of Low-Voltage DC Distribution Design.

Much like in a double-conversion UPS, a battery system is integrated at the 400/800 VDC level. The battery backup may be used for load smoothing, grid support, ride-through, backup power, or a mix of all three. Supercapacitors at the rack level may also be used for load smoothing, which could reduce the necessary battery capacity and/or extend battery lifetime. Batteries could also be installed at the rack level, as is done in the distributed UPS design. On-site inverter-based generation may also be connected to the LVDC network (rather than through its own set of AC/DC converters and step-up transformer). This could reduce losses and capital costs but may introduce operational complexities and reliability concerns relating to shared points of failure.

In principle, the motor drive rectifiers could also be eliminated by supplying the drive inverters directly from the LVDC distribution. However, rectifiers for drives are not necessarily major drivers for site-level cost or limitations. Commercial drive rectifiers may not be compatible with the DC supply conditions provided by the LVDC network, and otherwise beneficial drive features such as flying restart may become a source of complexity. Still, potential benefits from making the inertia of cooling motors available as a form of short-term energy storage (and savings in the form of reduced rectifier capacity and DC link capacitance) are worth further investigation.

¹Here, we use the term LVDC distribution to refer to distribution at DC voltages ranging from 600 to 4000 VDC. In datacenter industry literature, this is often referred to as HVDC. In this report, we delineate LV, MV, and HV levels within the context of electric power systems.

Design 5: Medium-Voltage Solid-State Transformer

Power density may be further increased beyond the LVDC design by replacing the MV to LV transformers and LVAC cables with a MV AC/DC converter and DC/DC conversion stage to step down the MVDC to LVDC. Solid-state transformer (SST) technology is viewed as a promising solution for achieving these functions (Figure 5).

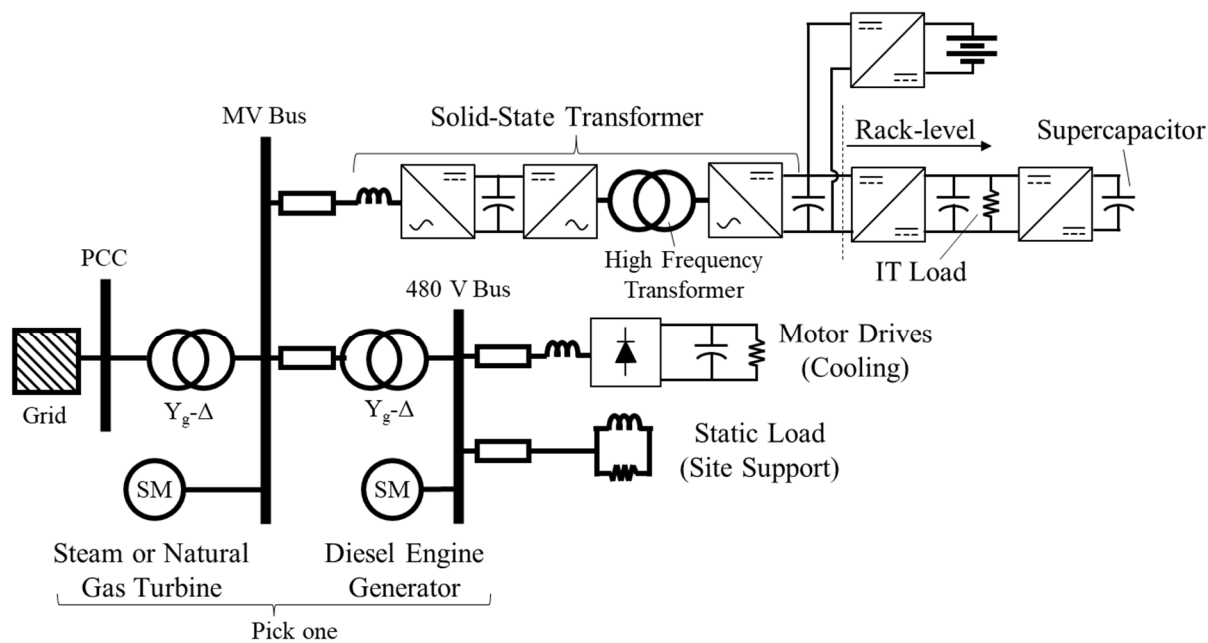


Figure 5: Single Line Diagram of Medium-Voltage Solid-State Transformer Design.

The SST replaces the MV to LV transformer and its output stage replaces the rack-level AC/DC converter employed in the LVDC distribution design—the SST directly provides the 400 or 800 VDC that is then distributed to the racks. The remaining downstream architecture is similar to the LVDC design. The number of racks that can be supplied with a single SST is uncertain given the ambitious R&D targets set in place for both SST deployment and AI rack power density. With a medium-voltage AC input, economical design of an SST rated for tens of MVA is plausible, meaning that a single SST will likely be able to serve more racks than the LV rectifier used in the LVDC distribution design.

For both the LVDC distribution and MVDC SST designs, improving the LVDC voltage to above 1 kV (e.g., 1.5 kVDC) has been identified as an R&D target. While this may require significant product development and improvements to personnel safety measures, the resultant changes from the perspective of EMT modeling may not significantly affect the aggregated model to be used.

Design 6: Medium-Voltage DC Distribution

The MVDC distribution design is the logical next step from the MVDC SST design—power density may be further increased by replacing the MVAC distribution with an MVDC distribution system (Figure 6). In terms of the scope of product development required, the MVDC design is a significant step involving cables, busbars, switchgear, circuit breakers, etc. to a much greater extent than in the LVDC distribution or MVDC SST designs. Thus, while data center suppliers

expect to begin deploying the LVDC and SST technologies in the field within the next several years, MVDC-based data centers are likely further away from seeing field service.

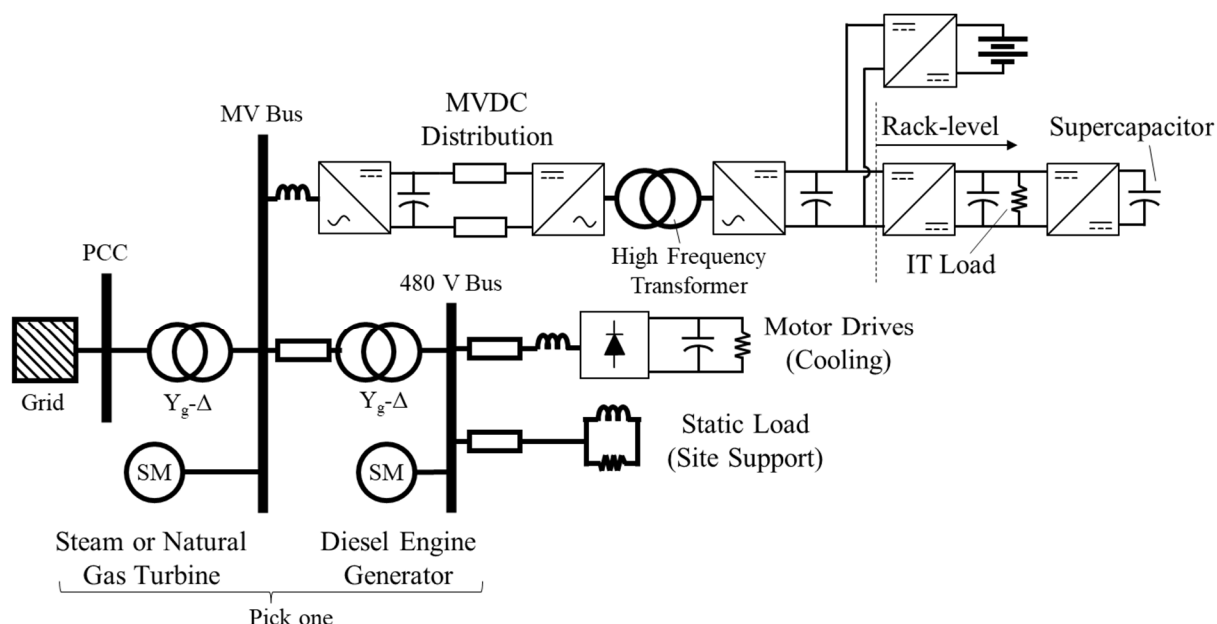


Figure 6: Single Line Diagram of Medium Voltage DC Distribution Design.

Observe that, from an aggregate modeling perspective, this is not radically different from the MV SST design—the primary difference is that the MV cable is now located after the MV AC/DC conversion stage; a high frequency transformer is still likely to serve as an attractive option for reducing MVDC to LVDC for rack-level distribution.

Table 1 summarizes the six data center designs introduced. Observe that evolution in data center power electronics is being driven by AI hyperscalers, and that future designs are trending towards the use of a 3 phase (PH) active front-end design, similar to that used in inverter-based resources (IBRs).

Table 1: Data center designs and their application and grid interface.

Design	Primary Application	ITE Grid Interface
1: Simple	Cryptomining	1 PH ITE Power Supplies
2: Centralized UPS	Modern data centers	3 PH active rectifier
3: Distributed UPS	Modern data centers	1 PH ITE Power Supplies
4: LVDC Distribution	Near-future (<5 yr) AI hyperscalers	3 PH active rectifier
5: MV SST	Near-future (<5 yr) AI hyperscalers	3 PH active rectifier
6: MVDC Distribution	Future (>5 yr) AI hyperscalers	3 PH active rectifier

For grid level studies, further simplifications of all these architectures may be possible—many grid-level studies of power electronics use highly simplified representations of any power conversion stages beyond those directly connected to the grid. In four of the six designs considered, the ITE equipment is interfaced with the grid via a 3-phase converter with energy storage. Further study and development of these converters may allow for existing modeling approaches for IBRs to be heavily utilized for representing data centers in grid-level studies. Early-stage performance requirements for large loads [17] [18] are similar in many respects to

IBR performance requirements, such as those in IEEE Std 2800 [19] and NERC PRC-029-1 [20].

Aside from emergent grid integration issues such as ride-through, designs 2 and 3 are highly mature from the data center perspective. Many data centers have highly stable electricity demand and use few or none of the high-power AI racks which are driving the power density requirements and investment in DC distribution systems. In such cases, designs 2 and 3 are attractive options, especially when reliability is paramount and thus appetite for less proven technology is lower. Thus, it is expected that these designs will continue to be used in a significant fraction of new data centers for the foreseeable future.

3.2 Balance of Plant

In Section 3.1, the topology of the HV, MV, and LV networks has been highly simplified in accordance with the DML's focus on grid-level studies. In this section, a brief description of AC HV, MV, LV networks in data centers is given so that DML users may be somewhat familiar with the detailed topologies that aggregated models are based on.

Generally speaking, the HV and MV power systems employed in large data centers are similar to those used in mission-critical industrial facilities or urban areas—numerous redundancies and alternate feeds are provided to accommodate faults and equipment outages. Space saving measures such as high-density substation layouts and switchgear are employed. Figure 7 illustrates two HV substation layouts sometimes used in data centers. These layouts are similar to distribution substations used by many utilities.

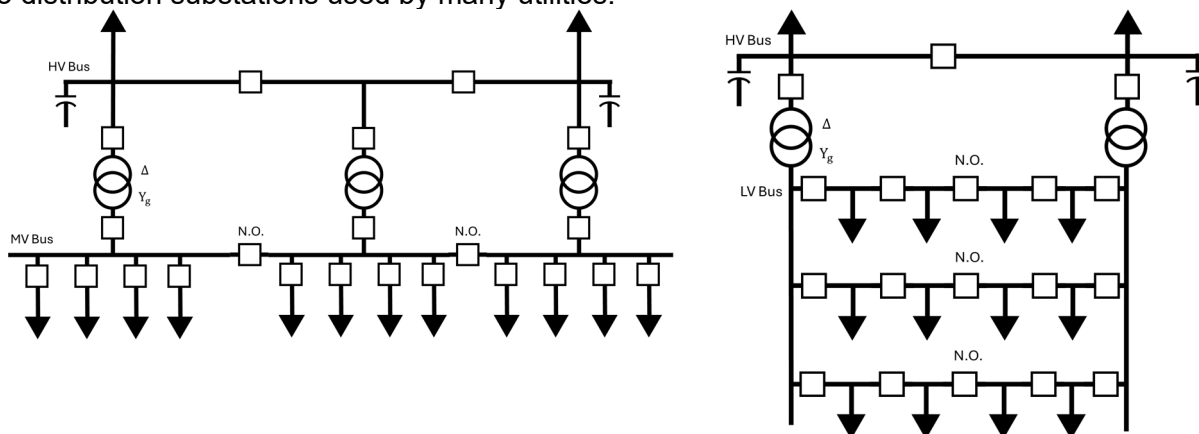


Figure 7: Exemplar substation layouts for data center HV substations.

The protection and control of these substations is also similar to typical utility practices; transformers and busbars are protected from faults using current differential protection. Short feeders may be protected either via time-inverse overcurrent or current differential. Large power transformers are equipped with mechanical protections and gas monitoring, and switchgear is equipped with arc flash protection.

Fast bus transfer schemes and networked distribution systems are less common as the UPS provide continuity of service to critical loads, reducing the need for the protection system to perform high-speed fault clearing or reconfiguration. That said, both automatic and manual reconfiguration schemes are widely used to ensure continuity of service even in the event of multiple outages or failures.

At the LV level, large data centers are often constructed by repeated “blocks” each rated for several megawatts each (Figure 8). Each block generally may be fed by two different MV feeds and, if backup generation is distributed (as is often the case), backup generation is connected (either at the MV or LV level). UPS are employed at this stage, often in redundant pairs and with each carrying a portion of the total load. In grid-level EMT studies, these UPS may be combined into a larger equivalent (this is the approach used in the DML examples). Cooling blocks also use UPS in larger data centers; the tolerance for cooling interruptions in hyperscale data centers is ever-decreasing as racks operate at higher power densities.

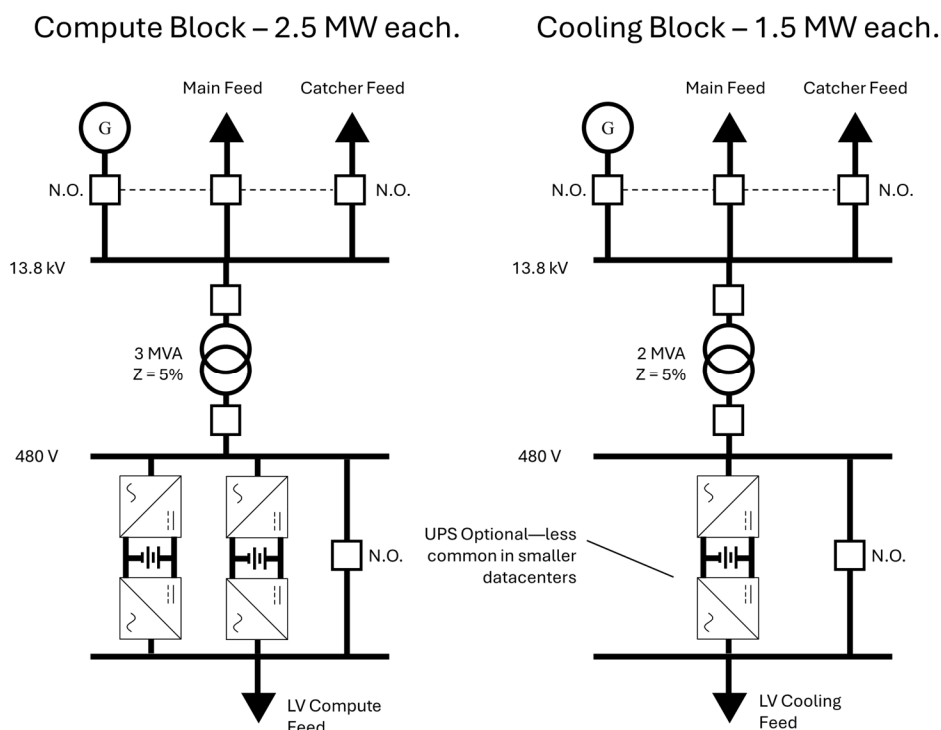


Figure 8: Single Line Diagrams for Medium-Voltage Compute and Cooling Blocks.

The low-voltage distribution equipment is then usually located within a dedicated electrical room located adjacent to the data hall where the ITE is located. Figure 9 illustrates the basic connectivity and arrangement of LV distribution equipment in relation to the data hall.

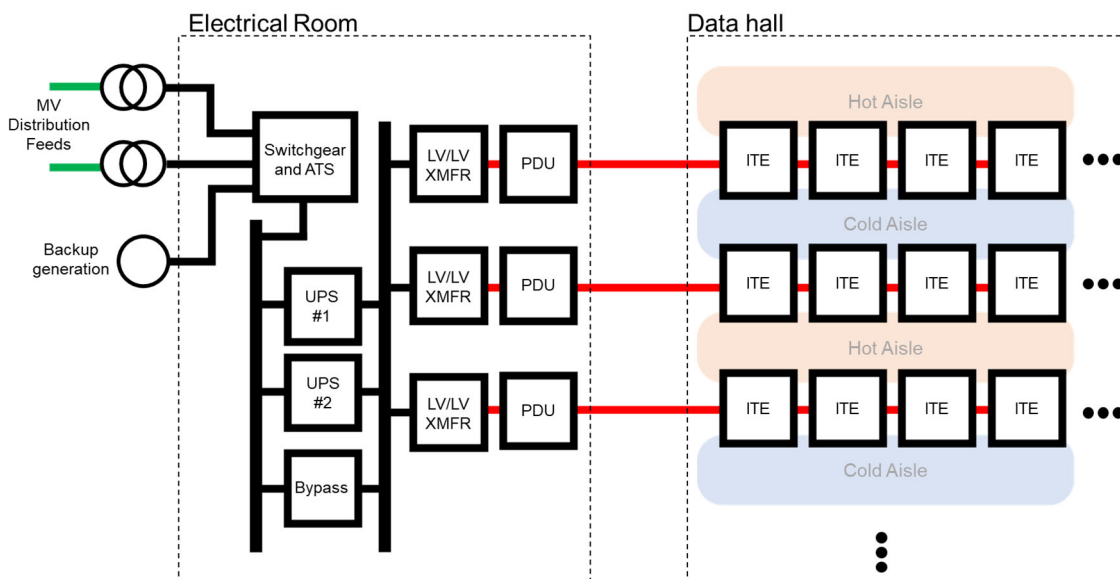


Figure 9: Simplified Layout of LV Electrical Distribution within Data Hall.

Power distribution units (PDUs) serve as switchboards for the LV cables feeding racks and are the primary means for monitoring and automation of power distribution at the rack level. PDUs range in functionality from basic high-quality power strips to automation and control platforms that provide high-fidelity monitoring and aggregation of a variety of electrical and mechanical sensory data from within the data hall. Thus, while PDU are a critical component of the site-level operations and monitoring, their relevance to grid-level EMT studies is limited.

Figure 10 and Figure 11 illustrate typical arrangements and installation conditions for LV distribution equipment in the utility room of a modern data center. Connections are usually made with cable located in metal conduit, with incoming feeds usually coming from MV equipment located outdoors and outgoing feeds running to the adjacent data hall. In high-density or space constrained sites, MV equipment may also be located inside.



Figure 10: Electrical Room Housing 28 MW of UPS Capacity [21].



Figure 11: Electrical Room for Medium-Sized Data Center [22].

Figure 12 and Figure 13 illustrate typical installation conditions within the data hall. Most of the floor space is dedicated to ITE racks. Both drop ceiling and raised floor are commonly employed to provide passage for air supplied by cooling-rack air handlers (CRAH), as well as potential passage for power cables, piping for any rack-level cooling, and communications cables.

Overhead raceways provide another path for routing this infrastructure. There are many different practices for how air flow and pipe/cable routing are handled at the data hall level [6].

As first indicated in Figure 9, ITE racks are arranged into rows and organized into hot and cold aisles. Rack-level cooling admits air from cold aisles and emits it into hot aisles; ports for user interactivity are located on the cold side of the rack and any hazardous high-power connections are located on the hot side. Some form of thermal barrier between aisles is generally used, Figure 13 illustrates the application of hot-aisle containment—the areas between aisles are enclosed in transparent panels and heat is exhausted through either the ceiling or floor¹.



Figure 12: Representative Data Hall [23]. This Facility is Rated for Tens of Megawatts, Tier IV Reliability, and LEED Gold Efficiency.

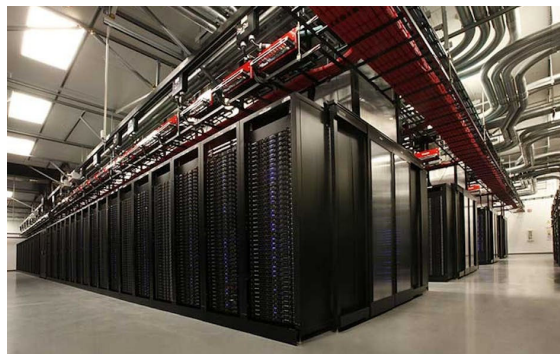


Figure 13: Representative Data Hall [24]. This Facility uses a High Power Density Design and Features Hot-Aisle Containment.

Figure 14 and Figure 15 illustrate typical installation conditions for the two main sources of cooling load, compute room air handlers (CRAH) (left) and chillers (right). CRAH are located in rooms adjacent to the data hall and provide the data hall with air that is regulated in terms of its temperature, flow rate, humidity, and pollution. The mechanical room usually houses automation controllers and support systems for both air and coolant handling. In large data centers, centralized chilled water plants are the primary method for rejecting heat produced by ITE² to the outside environment. Heat exchangers throughout the facility (e.g., with the CRAH and any rack-level liquid cooling) are dedicated to transferring heat away from ITE and into coolant loops that flow through outdoor chillers. In large data centers, plant-scale chillers are typically located on the facility rooftop.

¹Air flow velocities in data halls are usually too high for heat's natural tendency to rise to be a major design factor [6].

²The majority of electricity consumed by ITE is converted into heat. As a result of the thermal performance limitations of modern ITE and cooling systems, coolant temperatures are generally too low to support other processes (e.g., district heating or steam generation) [6]. However, market demands for higher power density are driving adoption rack-level liquid cooling solutions [106] and high-temperature semiconductors (e.g., SiC and GaN) [107]. These technologies permit higher coolant temperatures which may supply other processes.

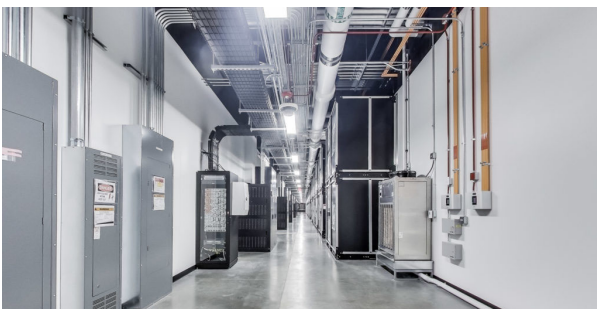


Figure 14: Mechanical Room Housing Compute Room Air Handlers (CRAH) [21].



Figure 15: Large Rooftop Chiller Unit for Data Center [21].

The pictured chiller is rated for 345 tons, meaning that the cooling water pump rating is likely about 1.5 MW. Large design margins are used when sizing cooling capacity, so the typical power demand for this chiller is likely to be significantly less than 1.5 MW.

4.0 Electromagnetic Transient Modeling of Data centers

In Section 2.0, as part of an overview of data center power systems, we have discussed some simplifications, common practices, and assumptions that may be employed to manage the potentially prohibitive level of detailed modeling involved in EMT modeling of large data centers, which contain tens of thousands of high-power components. As with many practical applications of EMT modeling, a clear understanding of study objectives and a series of pragmatic assumptions is required to complete studies in a reasonable time frame. In this section, we will discuss some potential applications for grid-level EMT modeling of data centers and the kind of EMT models that are suitable for conducting them. This discussion is aimed towards studies that consider the impacts of the data center(s) under study on the grid, rather than studies of site-level issues.

In subsection 4.1, general practices for determining the need and scope of EMT studies for data center interconnection studies are discussed. Subsection 4.2 addresses the applicability of the DML specifically to these studies.

4.1 EMT studies for Data center Interconnection

The details of EMT models are tailored to the kinds of study they are used for. In developing the DML, we considered a number of power system studies which might be conducted as a part of the data center interconnection process. The scope of studies discussed here is based on the scope of issues discussed in NERC's recent large load risk assessment [25] as well as a table developed by Electranix [26]. This overview is also informed by ongoing activities within the ESIG Large Loads Task Force and the NERC Load Modeling Working Group, both of which are developing data center modeling guidelines for grid-level studies. These will likely be publicly released in 2026.

Here, data center interconnection studies are organized into three categories: oscillatory interactions, voltage and frequency regulation, and power quality. This list omits studies which are clearly outside the domain of EMT analysis, such as load forecasting or evaluating steady-state capacity limits.

4.1.1 Oscillatory Interactions

The category of oscillatory interactions encompasses a wide range of scenarios, and the potential role of the data center and related modeling requirements varies. Figure 16 illustrates the essential elements of any oscillatory interaction, along with examples of the grid components and the elements they play a role in. Bolded and underlined items represent the data center components that can contribute to an oscillatory interaction. The current source with a series RLC circuit directly represents a circuit used to study harmonic resonance with shunt capacitors, but it serves as a convenient analog for other forms of oscillatory interaction.

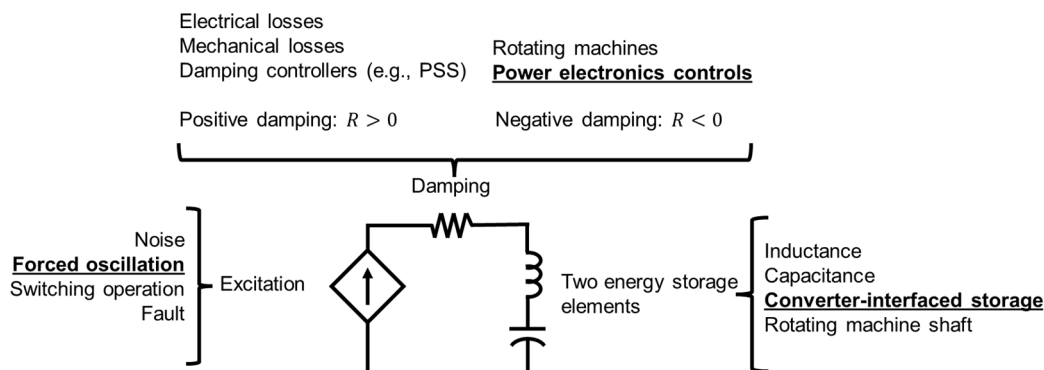


Figure 16: Essential Elements of an Oscillatory Interaction—Excitation, Damping, and at Least Two Energy Storage Elements.

Energy Storage Elements

Any oscillation involves energy exchange between at least two different forms of energy storage. The frequency of the oscillation is dictated by the time constants associated with the energy storage mechanisms. Purely electrical interactions (as opposed to electromechanical or control interactions) involve capacitors and inductors. Electromechanical interactions involve the kinetic energy stored in the masses of rotating machines. Even in the case of oscillatory interactions involving many devices (e.g., interarea oscillations), the devices involved can usually be lumped into one of two groups (e.g., the northern grid or the southern grid).

Damping

In the simple model of Figure 16, the energy storage elements are lossless—they exchange energy but do not cause any change in the total energy present in the system at a given time. The damping component represents the energy that is introduced or dissipated as energy flows between the two energy storage components. The total damping is the sum of the contributions from many devices, some of which introduce positive damping (i.e., they absorb energy) and some of which introduce negative damping (i.e., they supply energy). If the total damping is negative, any disturbance, no matter how small will result in instability (hence why “noise” is a valid source of excitation for an oscillatory interaction of concern). If an oscillation is lightly (and positively) damped, then the practical concern is that the oscillations produced by step changes (e.g., switching operations and faults) will be long-lasting and that oscillations produced by continuous inputs (e.g., noise or a forced oscillation) will have a large amplitude at certain locations in the system.

Component losses (e.g., mechanical friction, electrical resistance) are the main source of positive damping in power systems. Active components (e.g., rotating machines and power electronics) can provide either positive or negative damping and often produce a significant quantity of negative damping over some range of subsynchronous frequencies [27] [4] [28] [29]. In a real power system, the total damping is not the simple sum of that from individual elements but rather heavily affected by the network topology. The fact that a particular plant or load has negative damping is not inherently a problem—an individual device or plant may contribute negative damping (large or small) at subsynchronous frequencies and yet have a negligible impact on the total effective damping of a given oscillation¹.

¹In a recent Level 2 Alert, NERC has recommended that Transmission Operators should establish design requirements for Large Loads that ensures they are “designed in a way to increase damping of the listed

Excitation

Excitation introduces energy into the system, causing an oscillation. Its behavior is assumed to be independent of the system damping or dynamics of the energy storage elements, hence its depiction in Figure 16 as an ideal current source. The implementation of the excitation and its underlying assumptions vary based on the kind of interaction of concern:

1. Concerns that the net damping of a power system mode may be too low—in this case, the excitation may be a simple test signal, or methods which neglect excitation entirely (e.g., the use of transfer functions) may be employed.
2. Concerns that forced oscillations may attain high amplitudes (e.g., within a turbine shaft) and/or travel significant distances (e.g., due to the coincidence of the forced oscillation frequency with an interarea mode).
3. Concerns that intermittent disturbances may cause long-lasting oscillations

In practice, grid-level studies frequently make use of EMT simulation for (1), as this tends to be a less time-consuming approach to quickly screen for issues.

mode shapes for known power system oscillations” [109]. The majority of loads and generators connected to the power system do not and cannot meet this criteria—many will, theoretically, decrease the damping of subsynchronous modes. However, the effects are insignificant in the overwhelming majority of cases.

Table 2: Kinds of Oscillatory Interactions Data Centers Could Contribute to.

Phenomenon	Excitation	Negative Damping	Energy storage Element 1	Energy storage Element 2
SSTI due to forced oscillation exciting shaft modes	Data center load fluctuations with content in torsional frequency range (10 to 50 Hz)	N/A	Gas/Steam Turbine Shaft section	Gas/Steam Turbine Shaft section
Forced oscillation exciting interarea modes	Data center load fluctuations with content in interarea frequency range (0.1 to 1 Hz)	N/A	Group of rotating machines in one region	Group of rotating machines in another region
Forced oscillation exciting local modes	Data center load fluctuations with content in local frequency range (0.5 to 5 Hz)	N/A	Rotating machines at a specific plant	Rotating machines in the bulk grid
SSTI due to decreased damping of shaft modes	Noise/switching operation	Data center power electronics	Turbine Shaft section	Turbine Shaft section
SSCI between data center power electronics and other power electronics devices.	Noise/switching operation	Data center power electronics / IBR plant, HVDC line, FACTS device	Data center power electronics	IBR plant, HVDC terminal, or FACTS device
SSCI between power electronics and local generation plant	Noise/switching operation	Data center power electronics	Rotating machines at a specific plant	Rotating machines in the bulk grid
SSR due to negative damping from data center electronics.	Noise/switching operation	Data center power electronics	System series inductance	Series capacitor

4.1.1.1 Forced Oscillation Studies

In cases where the data center's load profile is the source of excitation—this is generally a concern for large data centers performing large-scale parallel compute tasks such as training or inference on large AI models—the data center load may be modeled using a user-defined time-varying current or power waveform, constructed using a time-series load profile provided by the data center developer [30]. The Fourier transform can be applied to the load profile to determine the affected frequency range (Figure 17).

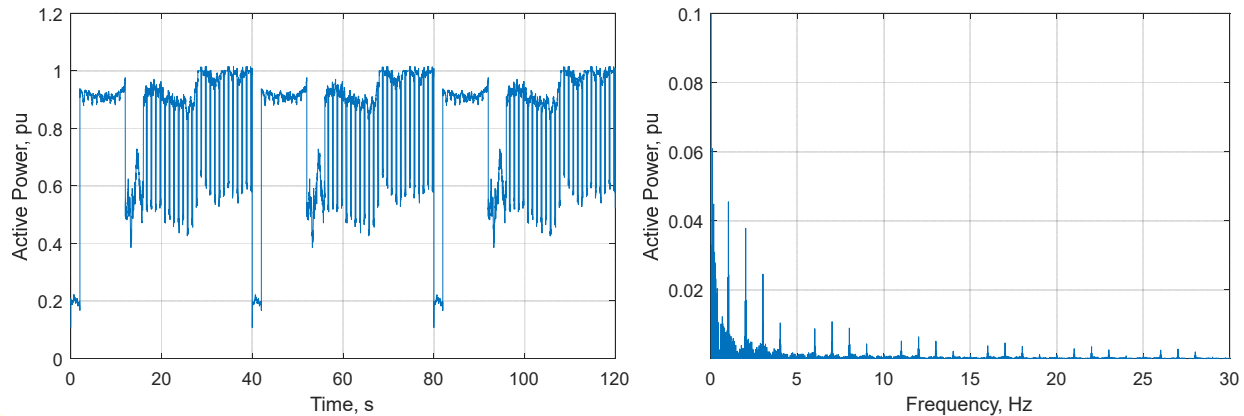


Figure 17: Exemplar Active Power Waveform for AI Training (left) and its frequency spectrum (right).

If there are negligible load fluctuations at frequencies above the bandwidth for which a utility's positive sequence transient stability models are designed, an EMT study is unlikely to yield additional benefits. Positive sequence transient stability models typically capture system dynamics accurately up to several hertz. Thus, EMT modeling is likely unnecessary for studying interactions between data center load fluctuations and electromechanical modes in the 0.1 to 5 Hz range. Rather, the primary reason to perform EMT modeling for forced oscillation studies is to evaluate effects on naturally occurring system modes in the 5 to 60 Hz range. This includes the torsional modes in large turbines, electrical resonances of series-compensated transmission lines, and modes associated with controls in grid-scale power electronics.

So far, EMT studies involving forced oscillations from data centers have primarily focused on the torsional modes of large turbines—the excitation of torsional modes is highly concerning as the torsional modes of gas and steam turbines tend to be very lightly damped, meaning that even a small torque oscillation at the stator terminals can result in a much larger (e.g., 20 to 40 times) torque oscillation between sections of the turbine shaft. The resulting twisting force on the shaft can lead to permanent damage to the shaft (e.g., in the form of permanent deformation and cracking) [31].

While the data center itself is novel as a source of forced oscillations with an unusual signature, practices for EMT modeling of the system and affected generators are mature and available in literature [32] [31] [27] [33]. Broadly speaking, the transmission system may be represented using relatively low-fidelity and most of the model's detail is directed towards the potentially affected component. Current gaps in industry understanding revolve around determining the ability of turbine generators to tolerate oscillatory loads on an ongoing basis [30]. Ultimately, such limits will require input from turbine OEMs, as only they have the design data and modeling tools necessary to determine the operating capabilities of their machines under these new operating conditions.

4.1.1.2 Small Signal Stability Studies

In small signal stability studies, the concern is that the data center may contribute a significant quantity¹ of negative damping to an oscillatory mode present in the power system (e.g., one of the last four scenarios described in Table 2). Examples of this include torsional interactions between steam turbines and controls used in LCC HVDC [28] as well as between turbines and and series capacitors [29] [27].

Unlike in a forced oscillation study, modeling the damping introduced by the data center requires a very detailed model—usually one that accounts for OEM- and model-specific variations in power electronics control. EMT analysis is usually used for small signal stability studies that involve oscillation frequencies too high to model accurately in phasor-based tools (e.g., >5 Hz).

The scope and modeling requirements for small signal stability studies can be difficult to define as the range of possible problems is so much greater than the range of problems which are practically relevant. While there do exist methods for system-level evaluation of small signal stability [34] [35], such methods are extremely arduous to scale up to practical power systems, requiring a deep understanding of linear system theory and hundreds of impedance scans. A single impedance scan of a detailed OEM-specific model can take several hours or even days to compute using a typical engineering workstation [36].

To manage the potentially broad scope of EMT small-signal stability studies, engineers often rely on recurring patterns from historical events to identify the need for such studies [37] [38] [25]. Indicators that EMT-based small-signal stability studies should be done include large concentrations of grid-scale power electronics (including HVDC terminals, FACTS devices, IBRs, and hyperscale data centers), series capacitors, and traditional generation [25]. The risk is typically higher when there are multiple such facilities present in a region that is weakly connected to the rest of the grid.

4.1.2 Regulation of Voltage and Frequency

While positive-sequence dynamic studies can represent most grid-level impacts that data centers can have on voltage and frequency regulation, there are specific situations where EMT analysis can be a helpful supplement². These situations usually arise when there is a need to establish confidence in the ability of simpler phasor-based models to represent grid-level impacts. Such situations include:

- Characterizing the fault response and ride-through performance of a data center that is based on vendor-specific solutions for achieving ride-through

¹Many common power system components such as generators, motors, and most power supplies introduce some amount of negative damping at the frequencies of existing oscillatory modes. In the majority of cases, such effects are negligible. Because of the significant effort and input data requirements associated with modeling this damping, careful engineering judgment is required when deciding whether to conduct a small signal stability study. The scenarios listed in Table 2 are derived from circumstances known previously to be a source of small-signal stability issues.

²Assuming that the EMT model itself is trustworthy, having been verified using experimental data and/or hardware-in-the-loop testing. This fact should by no means be taken for granted but is beyond the scope of this report to address.

- Assessing the performance of data center solutions for providing dynamic voltage or frequency regulation¹

For mature technologies and applications, where trust in the established phasor models is established, EMT modeling for these purposes is generally unnecessary. However, with data center power electronics evolving so rapidly, both in response to the needs of the grid and of the data centers themselves, significant work is still needed to establish the degree of conformance that data center power electronics have with recently developed phasor models for power electronics [39] [40] [41].

Lessons learned from IBR integration efforts are relevant here [42]—there are numerous instances of unintended vagaries, misapplications, and misunderstandings regarding performance requirements for power electronics which have led to grid disturbances. In other words, even if utilities have set requirements specifying that data centers perform in a way that they can capture using existing phasor models, there are likely to be many instances throughout the adoption phase where these requirements are not met. So long as the component-level power electronic models have undergone the appropriate validation, grid-level EMT studies can identify some of these instances before they result in real-world grid disturbances.

However, once one has confidence that the facilities in question can be adequately represented by the selected positive sequence model (e.g., the PERC1 model [39] [41]), the impacts on grid voltage and frequency regulation from data centers may be studied using phasor-based tools. Example studies include:

- Characterizing impacts to system voltage and frequency for a given data center ride-through characteristic.
- Determining the dynamic VAR margin and voltage stability limits for buses where data centers are connecting.
- Determining resource and frequency balancing resources needed due to data center ramping.

4.1.3 Power Quality

Technically, many power quality issues can be modeled using EMT analysis. However, it is often impractical to obtain input data with the quality needed to realize practical benefits over tools such as harmonic load flow software, short-circuit software, or engineering rules of thumb. From the level of grid-level power quality impacts from data centers, harmonics and voltage fluctuations are two important risks to consider [25].

Harmonics

Modeling grid impacts from data center harmonics can be broken down into two steps. The first step is the development of the data center's harmonic equivalent, usually given as either a harmonic current source or harmonic Thevenin equivalent. The second step is the evaluation of the voltage distortion produced in the grid. EMT modeling can theoretically be applied at the first step, but this is not recommended for reasons discussed shortly. EMT modeling is unnecessary

¹A recent subsynchronous oscillation event involving a data center was caused by weak grid conditions and a fast frequency response function present in the UPS [112].

for the second step, as a variety of commercial phasor-based programs support harmonic load flow¹ [43].

Serious practical obstacles arise when attempting to collect the data necessary to accurately model the harmonic spectrum of switching-based power electronics commonly used in data centers. Traditional sources of high current distortion (e.g., 30% current total harmonic distortion (THD)) include large diode rectifiers, single phase power supplies without PFC correction, and electronics-based lighting (e.g., fluorescent, sodium, or LED). Data center power electronics usually produce significantly less current distortion. For example, the Open Rack specification for 5 kW rack-level power supplies requires them to produce less than 5% current THD at 30 to 100% of full load [44]. Large double-conversion UPS produce around 3% current THD at full load [45].

The current distortion produced by switching-based power electronics is dictated by factors such as the converter topology (e.g., two-level versus multi-level modular, number of stages, interleaving), controller design and gains, PWM strategy, and parameters which can vary with the specific model of IGBT and/or MOSFET used (e.g., IGBT dead time [46]). These factors can vary significantly with device make and model, and even the data center designer is likely to find the level of modeling necessary to accurately reproduce the current spectrum through simulation to be excessive. Real-world harmonic spectrums obtained from either the field or the equipment OEMs are the most reliable sources of data [43].

Data center developers often develop and utilize standardized designs, and measurements taken from other data centers that are already in service and using similar equipment may be the best option available at the planning stage. Another reasonable approach is to collect sample current spectrums from electronics OEMs and aggregate the results using conservative assumptions (e.g., assume that current harmonics from different loads have the same or similar phase angle²).

4.2 Suitability of DML Specifically

In practice, it will seldom be the case that the example systems provided in DML can be used to study real data centers without significant modification. The primary value in DML comes from its potential to accelerate both community understanding of how data centers should be represented in grid-level studies and in the development site-specific EMT models.

Utilities and consultants may find the DML models instructive for understanding the general dynamics of data centers, and for exploring the suitability of various technical solutions for

¹Specific utility requirements may not always be consistent with this view [17]. In such cases, follow-on discussions should consider applicable practices and guidance published by consensus-building organizations such as the IEEE, NERC, and E-SIG, all of whom are developing guidance in these areas at the time of writing.

²Treating the individual load harmonics as in-phase may be excessively pessimistic. Field experience with harmonic currents injected by IBRs indicates that the aggregate harmonic distortion is roughly the square root of the sum of the squares of individual units [36]. For example, if 1 inverter contributes 1 A of harmonic current, then 100 inverters would contribute 10 A of harmonic current. Similar rules of thumb could apply to data center power electronics.

meeting grid requirements relating to ride-through and SSO. Data center developers and OEMs of data center equipment may find these models instructive for understanding which aspects of their highly sophisticated systems are of most importance for grid-level studies, and examples of how their equipment is represented in grid-level studies. DML component models may serve as starting points for OEM- or site-specific EMT models, which many utilities are beginning to request as part of the interconnection process.

5.0 Model Overview

This section provides an overview of the models included in the library, including their major design features and intended uses. We focus on explaining the reasoning behind the model design decisions, including both background on data center design and major assumptions. For component-by-component descriptions of the models, refer to Section 6.7.4.

For precise specifics of how model functions are implemented, users should refer to the accompanying PSCAD files—there is no obfuscation of the model functionality (i.e., there are no black-boxed or encrypted components), and the model schematics have been organized and annotated so that EMT program users can readily interpret the models and adjust them for their own needs.

The DML contains 37 component definitions and 10 simulation files. The component definitions provide modular representations of commonly-used components or functions and are the primary contribution in terms of modeling effort saved for the user. The simulation files are example power systems that demonstrate proper use of the component definitions, primarily by illustrating their use to represent the six archetypical data center designs described in Section 2.0.

Table 3 lists the complete power electronic device models included in the DML and their purpose. In addition to the power electronic hardware, these components contain any additional passive components and control algorithms necessary for the device to be useful for grid-level studies. These are the most sophisticated components in the library, with most of the other components supporting these.

Table 3: Complete Power Electronic Device Models included in the DML.

Model	Definition Name	Purpose
DC-DC Buck-Boost Converter (AVM)	DC_bi_avm	Interface DC devices (e.g., batteries, supercapacitors) with inverters (e.g., UPS) (AVM)
DC-DC Buck-Boost Converter (SWM)	DC_bi_swm	Interface DC devices (e.g., batteries, supercapacitors) with inverters (e.g., UPS) (SWM)
3 PH Inverter, GFL	inv_gfl	Three-phase inverter with GFL control (e.g., UPS rectifier or grid interface for DC distribution designs) (AVM)
3 PH Inverter, GFM, Droop Control, SWM	inv_gfm_droop_swm	Three-phase inverter with GFM droop control (e.g., UPS output inverter or grid interface for DC distribution designs) (SWM)
3 PH Inverter, GFM, Droop Control, AVM	inv_gfm_droop_avm	Three-phase inverter with GFM droop control (e.g., UPS output inverter or grid interface for DC distribution designs) (AVM)
3 PH Set of 1 PH Rectifiers	rect_3x_full_wave	Simplified representation of small motor loads (e.g., fans)
3 PH Set of 1 PH Rectifiers with Protection	rect_3x_full_wave_c	Simplified representation of small motor drive loads (e.g., fans) with built-in voltage protections
3 PH Diode Rectifier	rect_six_pulse	Simplified representation of large motor drive loads (e.g., rooftop chillers)
Variable freq. drive, AVM	vfd_avm	Medium-size drive-based cooling loads such as centrifugal pumps for chillers (AVM).
Variable freq. drive, SWM	vfd_swm	Medium-size drive-based cooling loads such as centrifugal pumps for chillers (SWM).
Variable freq. drive, AVM, 1PH	vfd_avm_1PH	Small drive-based cooling loads such as centrifugal fans (AVM).
Variable freq. drive, SWM, 1PH	vfd_swm_1PH	Small drive-based cooling loads such as centrifugal pumps (SWM).
1 PH Rectifier with PFC, SWM	pfc_swm	Grid interface for rack-level power supplies (SWM)
1 PH Rectifier with PFC, AVM	pfc_avm	Grid interface for rack-level power supplies (AVM)

Table 4 lists the control algorithm components provided in the DML. These are mostly commonly employed control elements for power electronics and are used in the complete power electronics device models.

Table 4: Control algorithm components included in the DML.

Model	Definition Name	Purpose
GFM Droop Control	gfm_droop	Primary control structure for GFM droop control
<i>dq</i> -Domain current regulator	ireg	Provides current control for inverters with multi-layer controls
<i>dq</i> -Domain Current Limiter	ilim_dq	Provides current limiting for inverters with multi-layer controls
PI Controller with Anti-Windup Logic	PI_AntiWindUp	Improvement over standard PI controller to include anti-windup functions commonly used in inverters
Stabilizer for Droop-Based GFM Control	stage2_ilim	Supplementary control for droop-based GFM control to improve stability during/after faults
<i>dq</i> -Domain Voltage Regulator	v_reg	Provides voltage control for inverters with multi-layer controls
GFM Droop Control	gfm_droop	Primary control structure for GFM droop control

Table 5 lists grid components included in the DML. This includes two simplified LV cable models, intended to provide reasonable cable representation without the large input data requirement associated with a cable constants routine, as well as a reciprocating engine generator model.

Table 5: Grid Components Included in the DML.

Model	Definition Name	Purpose
Lumped LV Cable, 1 PH	LV_cable_1PH	Simplified low-voltage cable model with minimum input data requirements (single phase)
Lumped LV Cable, 3 PH	LV_cable_3PH	Simplified low-voltage cable model with minimum input data requirements (three phase)
Recip. Engine Genset	gen_recip	Reciprocating engine gensets used to provide standby or bridging power for large data centers.

Table 6 lists load profile components provided in the DML. These are used to simulate rapid variations in active power demand associated with large-scale parallel computing processes.

Table 6: Load Profile Components Included in the DML.

Model	Definition Name	Purpose
Variable AI Training Load	load_ai_train	Highly simplified square-wave model for AI training load, useful for exciting target frequencies
Playback-Based Electronic Load	load_playback	Read in an external active power profile from .csv file, also supports simplified controls for LVRT

Table 7 lists the power electronics hardware components included in the DML. Of all the devices covered by the complete power electronics models (Table 3), the hardware-only

component definitions include only the 3 PH inverter models as only these were considered sufficiently complex to merit organization of the hardware into a standalone definition.

Table 7: Power Electronics Hardware Components Included in the DML.

Model	Definition Name	Purpose
3 PH Inverter, AVM	VSC_AVM	Hardware for three-phase VSC with optional device-level current limiting (AVM)
3 PH Inverter, SWM	VSC_SWM	Hardware for three-phase VSC with optional device-level current limiting (SWM)

Table 8 lists protection system components included in the DML. These are used to implement various load-level protections that trip off elements of data center load in response to grid disturbances (usually voltage sags).

Table 8: Protection System Components Included in the DML.

Model	Definition Name	Purpose
UPS Controller	ups_ctrl	Centralized controller for UPS to handle protection tripping and transitions between modes
3 PH Contactor	uv_sw	Three-phase contactor with voltage protections
1 PH Contactor	uv_sw_1PH	Single-phase contactor with voltage protections
Generator Autosynchronizer	gen_sync	Synchronize a generator with a grid prior to circuit breaker closing.

Table 9 lists signal processing components included in the DML. These implement commonly-used signal processing functions and are used throughout other components and system models in order to improve organization and usability.

Table 9: Signal Processing Components Included in the DML.

Model	Definition Name	Purpose
dq-Domain Power Calculation	PQ_dq	Compute active and reactive power in dq domain
Per-unit Base Calculator	pu_bases	Compute derived bases for convenient per-unitizing
Unbalance Calculation	unb_rms	Compute voltage unbalance per ANSI 47

The following subsections are dedicated to discussing the approach and reasoning behind the selection of these specific component models to represent the variety of equipment present in data centers. For discussion of the site-level design, refer to Section 2.0.

5.1 IT Loads

The demand associated with ITE is a majority of data center electricity consumption and may be subdivided into three categories:

1. Compute load, which is dedicated to running processors (e.g., general-purpose central processing units (CPUs), GPUs, or application-specific integrated circuits (ASICs)) which perform a broad range of computationally intensive tasks.
2. Storage load, which is dedicated to storing and retrieving data on non-volatile storage media such as hard drive disks (HDDs), solid-state drives (SSD), and tape storage systems.
3. Communications load, which is dedicated to routing information in, out, and throughout the data center. Common devices include routers and ethernet switches.

Compute load tends to be the dominant source of electricity demand. It is also the most variable with respect to the site's end use (e.g., providing cloud services vs. mining cryptocurrency).

As outlined in Section 3.1, the electrical interface between the ITE and grid can differ substantially depending on the power electronics architecture adopted by the data center. Today, most data centers use Design 2 (centralized UPS) or 3 (distributed UPS), with the former being more common. As a result, the grid-level dynamics of much data center ITE is determined by the behavior of large 3 PH UPS—these are the focus of the next subsection. In the remaining subsections, we discuss the modeling of the ITE power supplies themselves, the nature of variations in data center power demand that are relevant on an EMT timescale, and the implications of evolving DC distribution architectures (Designs 4, 5, and 6) on grid-level modeling of ITE.

5.1.1 Uninterruptible Power Supplies

Reliability has long been, and in many cases still is, the primary performance requirement for data centers (with energy efficiency and cost being secondary considerations) [6]. Thus, uninterruptible power supplies (UPS) are widely used and, in many cases, may be considered the most significant component when it comes to defining a data center's dynamics from the perspective of a grid-level EMT study. For example, when utilities and data center operators discuss improving data center ride-through, it is often the protection settings and tolerances of the UPS that are the primary focus of technical discussion.

Large data centers usually use large three-phase UPS, which tend to be rated for roughly 1 MVA each and use a double-conversion design (Figure 18):

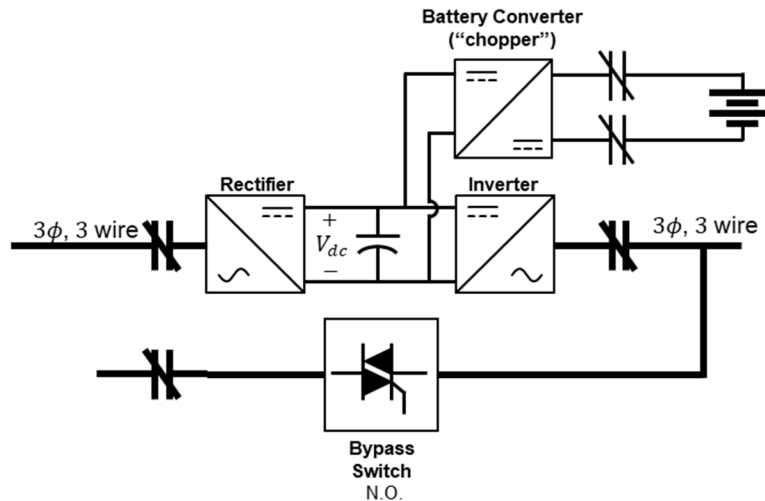


Figure 18: Major Components of Double-Conversion UPS.

The AC output voltage of the UPS is tightly regulated, generally varying in magnitude by less than a few percent even during full load pickups [45] [47]. Consequently, grid disturbances tend to have little influence on the AC output voltage or current, and it is generally unnecessary to model equipment downstream of a double conversion UPS for a grid-level EMT study.

Other well-known UPS technologies include line-interactive or rotary UPS, but these are far less common in large data centers than the double conversion design. Double conversion UPS generally provide the greatest degree of protection for the load (and thus the most significant benefits for site reliability), and improvements in its cost and efficiency over time made it generally the most competitive of the UPS technologies for data center applications.

From a grid perspective, the rectifier and its controls are the most influential in determining the UPS's response to disturbances, although the other two converters also play a significant role during voltage excursions. Rectifiers for the large, three-phase UPS used in data centers are generally three-phase voltage-source converters; modern designs usually use a three-level converter (either I- or T-type) [48] [6] or a Vienna rectifier [49] [50]. Diode rectifiers are virtually extinct in modern double conversion UPS; they provide neither the efficiency nor the DC link voltage regulation that modern applications demand.

While EMT modeling of existing data centers may consist primarily of double-conversion UPS modeling, this may change in the near future. Attitudes towards reliability in AI data center applications are not necessarily aligned with historical applications, and philosophies are mixed among designers today. Capital costs associated with large data centers are significant (e.g., over \$10B for a 1 GW facility [51]) and backup generation and UPS are a nontrivial component of this cost. As data centers grow larger, they are connecting to higher-voltage substations which experience fewer interruptions and milder voltage sags. Several data center topologies (e.g., designs 3, 4, and 5 in Section 3.1) look to incorporate significant energy storage downstream of UPS. Therefore, the ubiquity of the double-conversion design should not be taken for granted, especially for newer installations.

Scope of DML Components

In the DML, components for a double-conversion UPS are provided (Figure 19).

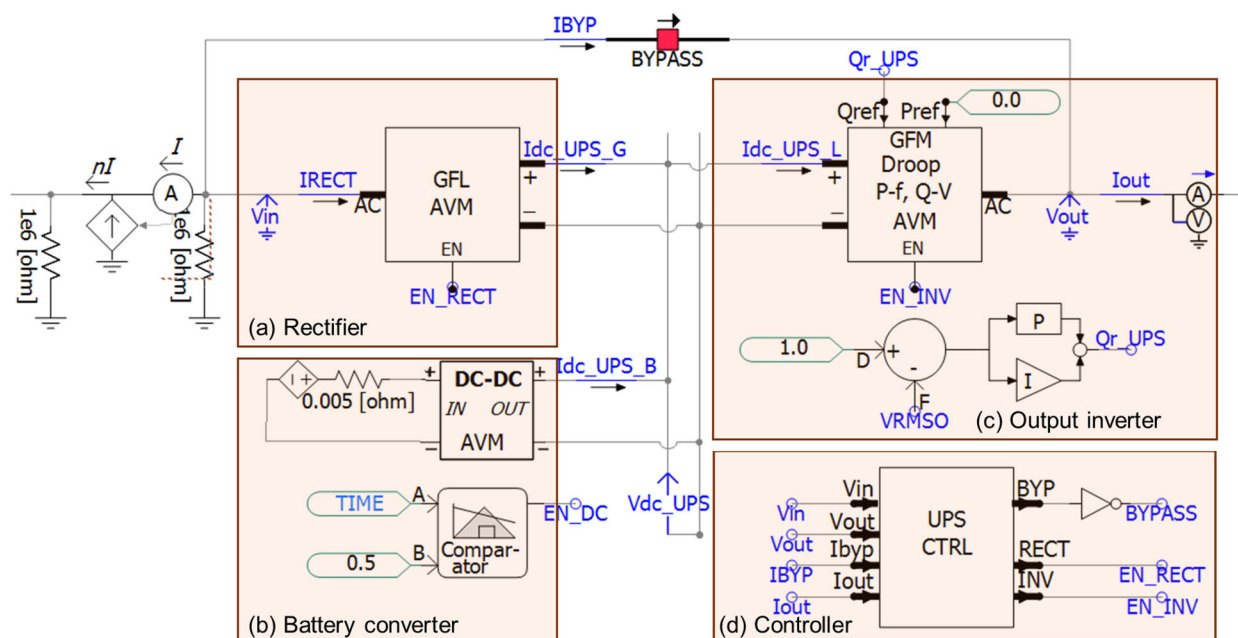


Figure 19: Use of DML Components to Represent 3-Phase Double-Conversion UPS.

The rectifier is represented as an inverter with GFL control (`inv_gfl`) with controls typical of an inverter configured to provide minimal grid support. It operates at unity power factor and regulates the DC link voltage. A switching model (SWM) for a basic two-level 3 PH inverter is provided (`inv_swm`), but SWM for more advanced (and common, in the case of large 3 PH UPS) designs such as T-type inverters or Vienna rectifiers are not provided. Such designs use sophisticated switching strategies that, while they enable the higher efficiency these designs provide, have relatively minor impacts on grid-level dynamics. Generic models, such as those provided in the DML, do not offer the precision necessary to capture these impacts—OEM-specific models should be used to address concerns related to specific inverter topologies.

The battery converter is modeled as a bidirectional buck-boost converter (`DC_bi_avm`) and has two control loops—a slow power regulator which represents battery charging control and a fast DC voltage regulator which is designed to rapidly increase the battery output in the event of a small DC link voltage sag. Such a sag indicates that the rectifier has either been tripped offline or hit its current limit (e.g., due to a grid-side voltage sag) and thus the battery converter steps in to avoid any disruption to the load.

The output inverter is represented as a grid forming (GFM) inverter (`inv_gfm_droop_avm`) with droop control. A fast AC voltage regulator is added as an outer loop control to minimize AC voltage magnitude fluctuations during large load changes. A relatively high current limit (1.5 pu) is used, a common design practice which allows the UPS to be used for transformer energization and motor starting [45] [47]. Average-value models are used for all three power converters.

UPS protections and transitions between modes are implemented within a separate UPS controller block (`ups_ctrl`). Basic AC voltage protections are present. The UPS may be started in normal, bypass, or battery backup modes. The UPS load is modeled using an AI training load component (see `load_ai_train` and `load_playback`).

5.1.2 ITE Power Supplies

ITE and the peripherals that support them (e.g., metering and fans) generally accept power at 5 to 50 VDC and so require an AC/DC power supply to interface with the grid. For grid-level EMT studies where power electronics are explicitly modeled, the power supplies for the IT load should be represented if they are directly connected to the grid. This commonly occurs in one of two scenarios:

- 1) There is an upstream UPS which is operating in bypass/eco-mode¹
- 2) UPS functionality is provided at the rack level (e.g., via a battery connected to the low-voltage DC output from the IT power supply)

If the data center IT load is connected to the grid through a double-conversion UPS, the AC voltage seen by the IT load will be very tightly regulated and the IT load itself can be modeled as a simple current source or passive load.

Technical performance guidelines for data center power supplies are defined under the OpenCompute [52], but a single power supply design is not prescribed. There are a wide variety of single-phase power supply designs used to power IT equipment. At the scale of large data centers, single phase power supplies are rated for several kilowatts each and use some form of PFC, meaning that they produce relatively low levels of current harmonics. Roughly speaking, most power supplies can be represented using the simplified diagram shown in Figure 20.

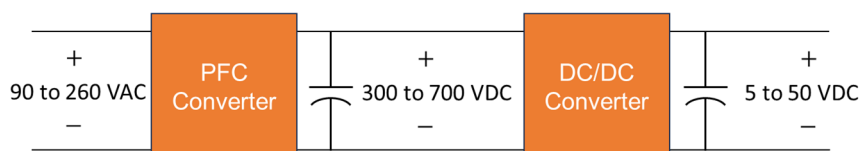


Figure 20: Simplified Power Supply Diagram with Notional Voltage Levels.

The PFC converter converts AC to DC and performs PFC, which, for a power supply, primarily involves reducing harmonic currents. To obtain good efficiency, the PFC converter generally operates in a boosting mode, meaning that the DC voltage must exceed the AC voltage and the DC output voltage is generally several hundred volts. A DC/DC conversion stage is then necessary to significantly reduce this voltage to one suitable for electronics—low power consumption devices such as personal computers generally accept 5 or 12 VDC whereas 48 VDC is used for power-dense racks in data centers. The DC/DC converter also generally provides galvanic isolation (most commonly with a transformer) in order to minimize the coupling of noise from the high voltage stage into the low voltage stage where it may harm downstream electronics.

For the purposes of grid-level studies, representation of the PFC converter is the most important, and representation of the DC/DC converter and other downstream equipment is generally heavily simplified. PFC converter designs can be broadly categorized as either unidirectional or bidirectional. Figure 21 illustrates common variations of unidirectional PFC converters [53]. The conventional design (the leftmost) is seldom used in modern data centers owing to its lower efficiency; the bridgeless and totem-pole designs are essentially two different approaches for reducing the number of semiconductor switches in series.

¹Bypass mode is generally used when an individual UPS is out-of-service for maintenance or repair and so is not represented in an aggregate data center model.

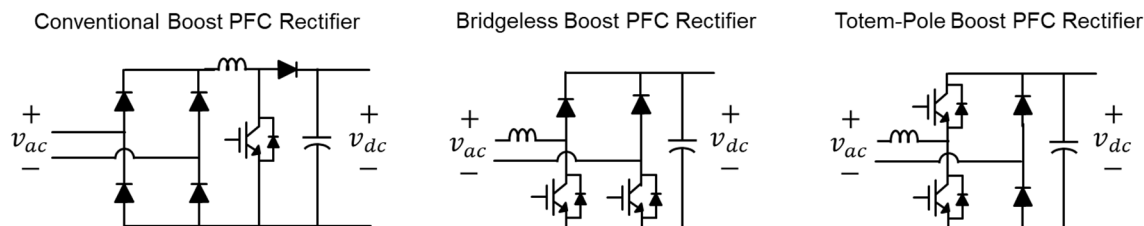


Figure 21: Common Variations of Unidirectional PFC Converters.

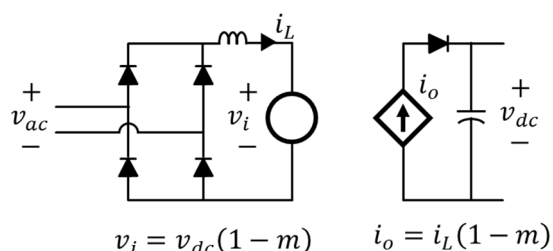


Figure 22: AVM for Unidirectional Boost PFC Rectifiers.

MOSFETs may obtain significantly lower forward voltage drop than diodes (e.g., 0.2 V vs. 0.7 V) and further efficiency improvements are realized by replacing the remaining diodes in the PFC rectifier with MOSFETs, resulting in a single-phase voltage source inverter (Figure 23), which is bidirectional. This approach is popular in high-performance power supplies not because of the bidirectionality or control flexibility but simply due to the efficiency gains. Generally, efficiency is the primary indicator of a power supply's sophistication and cost, and IT power supplies in large data centers operate at efficiencies in the range of 96 to 99%. Small efficiency gains in this range are impactful not necessarily due to reduced electricity costs but due to the reduced heating, which allows for higher power density and reliability (e.g., improving efficiency from 96% to 97% corresponds to a 25% reduction in heat produced).

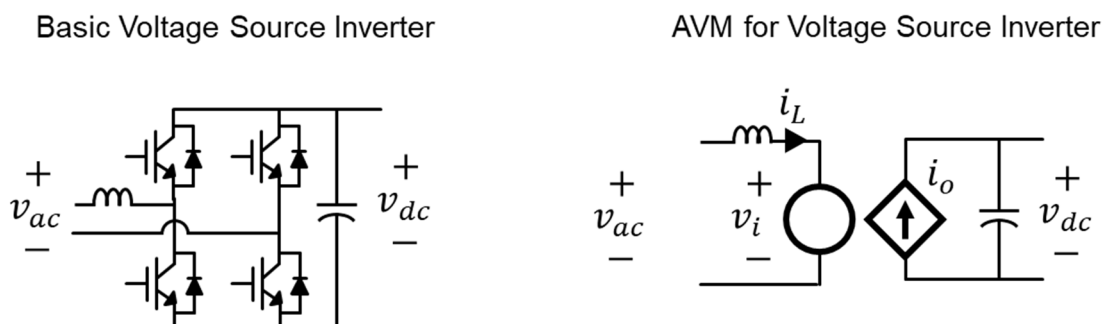


Figure 23: Basic Voltage Source Inverter Topology (Left) and its AVM (Right).

It is common for the two switching legs to use different devices—one leg is optimized to minimize switching losses and performs pulse-width modulation (PWM) while the other is optimized to minimize conduction losses [54]. The latter leg switches only once every half cycle, playing the same role as the diodes in the totem-pole converter. In other words, while the single-phase voltage-source converter (VSC) is capable of four-quadrant operation (and thus a variety of grid support functions), in PFC converter applications it is operated at unity power factor and only consumes active power.

In addition to the basic two-leg design shown in Figure 23, more sophisticated topologies are used to obtain higher efficiency and better power quality (e.g., [55] or [56]). However, for grid-

level studies, the conventional average-value model (AVM) for a single phase VSC (Figure 23) may often be used to represent these topologies, and efforts to improve PFC converter model fidelity for grid level studies should focus primarily on representing variations in closed-loop control design, rather than different topologies. The SWM of many modern power supplies are impractical to model in EMT studies as they tend to employ switching frequencies well above 100 kHz. Thus, variations in hardware that do not affect the converter's AVM are unlikely to be meaningful for grid-level studies.

Further work is needed to investigate the role, if any, that the DC/DC converter models should play in grid-level studies. Two common designs for the DC/DC conversion stage are the high-frequency transformer or LLC converter [57]:

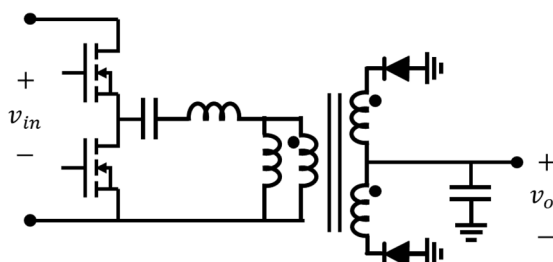


Figure 24: Schematic of Basic LLC Converter.

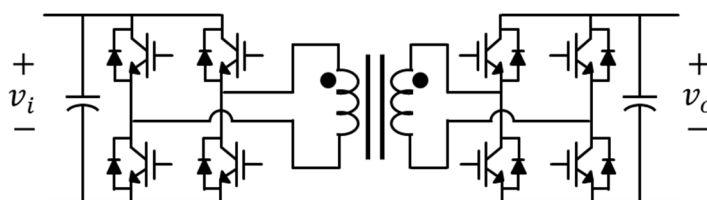


Figure 25: Schematic of High Frequency Transformer for DC-DC conversion.

Both large- and small-signal response of these designs should be investigated. The large signal response is primarily relevant for grid fault studies—if grid faults cause significant fluctuations in the DC/DC converter's input voltage, the dynamics of the input current should be evaluated. A simple constant current or constant power source with a first-order low-pass filter may suffice. The converter's small-signal response is primarily relevant for studies of oscillatory interactions, as discussed previously in Section 4.1.1. The importance of the DC/DC converter in such cases should be evaluated by injecting small subsynchronous oscillations at the terminals of the PFC converter and evaluating its small-signal input impedance. If modeling the DC/DC converter dynamics significantly affects the input impedance, then it should be considered in SSCI studies.

As with the PFC converter, there are many multi-stage and interleaved variations of both the high-frequency transformer and LLC converter [58] [59] [60], which permit higher efficiency and power density. It is plausible that these variations will be unimportant for grid-level studies, but some investigation is necessary.

Scope of DML Components

In the initial release of DML, two single-phase power supply models are included:

1. A conventional PFC boost rectifier SWM (`pfc_swm`)

2. A PFC boost rectifier AVM, which represents an AVM for a variety of unidirectional PFC converters (e.g., those three shown in Figure 21) (`pfc_avm`).

These models were developed based on models of power supplies of cryptomining hardware [61], which are also now publicly available [62].

Inclusion of a single-phase inverter model is a priority for the next round of development—the single-phase inverter design is particularly useful for studying solutions for improving grid stability, as it is far more capable of providing grid support functions (e.g., fault ride-through or dynamic reactive power support) than the unidirectional designs. The SWMs—items (1) and (3) above—are included primarily to allow for validation against the corresponding AVMs. In the interim period, users may consider the basic 1 PH inverter model provided by Manitoba Hydro as a starting point [63].

While there are a wide variety of hardware topologies and PWM switching strategies for both unidirectional and bidirectional PFC converters [64] [56]. Most such variations have little influence on the power supply's AVM, and the SWMs included with the library are included to serve as benchmarks for the AVMs—the AVMs should be used for grid-level studies as they allow for a much larger simulation timestep (50 μ s vs. 5 μ s). Notably, harmonic studies are an exception to this guideline. Variations in hardware topology and modulation strategy are massively influential on the power supply's harmonic spectrum, but so are factors which are impractical to include in grid-level EMT models, such as the specific MOSFET selected by the OEM. Harmonic spectrums for power supplies should be obtained through testing, field measurements, and/or support from the OEM, rather than through EMT modeling.

5.1.3 Short-Time Load Profiles

In this section, we discuss the causes and nature of rapid load fluctuations in data centers which can be relevant for EMT studies. This context will help DML users to create more realistic scenarios with their models—DML components have built-in functions to represent many of the data center behaviors discussed here.

The active power demand of some aggregate ITE can vary significantly on a timescale relevant to EMT studies (i.e., it can vary quite rapidly). This makes it necessary to apply a time-varying load to the IT power supply model for certain kinds of data centers. Most data center ITE operates at very nearly unity displacement power factor, and most reactive power flow arises from balance of plant equipment such as transformers, harmonic filters, and shunt capacitors.

Until the past few years, data center loads have been generally regarded by grid operators as stable, smooth, and dependable [65] [66]. While electronic power supplies and UPS have both long been capable of quickly ramping, the sheer variety of sectors and applications making use of data center services resulted in the individual compute, storage, and communications loads within most data centers being highly uncorrelated with one another or even factors which most types of load covary with significantly, such as the time of day or week. The result is very consistent electricity demand, with no meaningful fluctuation on the timescales associated with EMT modeling. Three factors have contributed to a shift in this view:

1. Cryptomining
2. Increased scrutiny over data center tripping

3. Hyperscale parallel computing processes

Short-Time Demand Variations from Cryptominer Demand Response

In the case of cryptomining, short-time load variations are driven by fluctuations in the price of electricity and electricity incentives, which can comprise a significant fraction of the facility's total revenue in some markets [67]. In the absence of ramping requirements, large cryptomining facilities may significantly vary their load in response to changes in power market conditions [68]. Traditional data center business models heavily prioritize reliability and uptime—they seldom participate in demand response programs.

Short-Time Demand Variations from Data Center Tripping

Traditional data center applications are not known for quickly ramping online or rapidly varying their workload; minimizing risk to site processes is a major priority in how the data center is operated and transitions back to grid power are handled carefully. However, in recent years, both traditional data centers and cryptominers have come under scrutiny for their tendency to disconnect in response to brief voltage sags [69] [70] [71]. The systemic nature of this behavior at these facilities has resulted in unexpected gigawatt-scale load drops and effects measurable at the interconnection level.

The ride-through behavior of a facility's ITE (the majority of its load) is driven by three factors, the applicability of which depends on the design of the site's protection system

1. Site-level undervoltage protections, potentially implemented in protective relays installed at the HV, MV, or LV levels. These may be part of automatic transfer schemes that control separation from the utility and the transfer to on-site generation.
2. Protections within rack-level power supplies: During a grid-side voltage sag, the response of most PFC converter controls will be to consume additional current in order to maintain the DC bus voltage (i.e., the power supply exhibits a constant power characteristic). There is usually overcurrent protection present so that, if the current increase is excessive, the PFC converter is tripped offline. However, the PFC converter may have a current limiting control, in which case the converter reverts to constant current behavior for deep voltage sags. The DC bus voltage will then decline over time, as the converter is no longer drawing sufficient power from the grid to offset the energy consumed by the load. In this case, the PFC converter may eventually trip on DC bus undervoltage. Some PFC converters use AC undervoltage protection as well. Figure 26 illustrates one potential response of a PFC converter to an AC voltage sag, with annotations indicating elements of the PFC response that may trip protection functions.

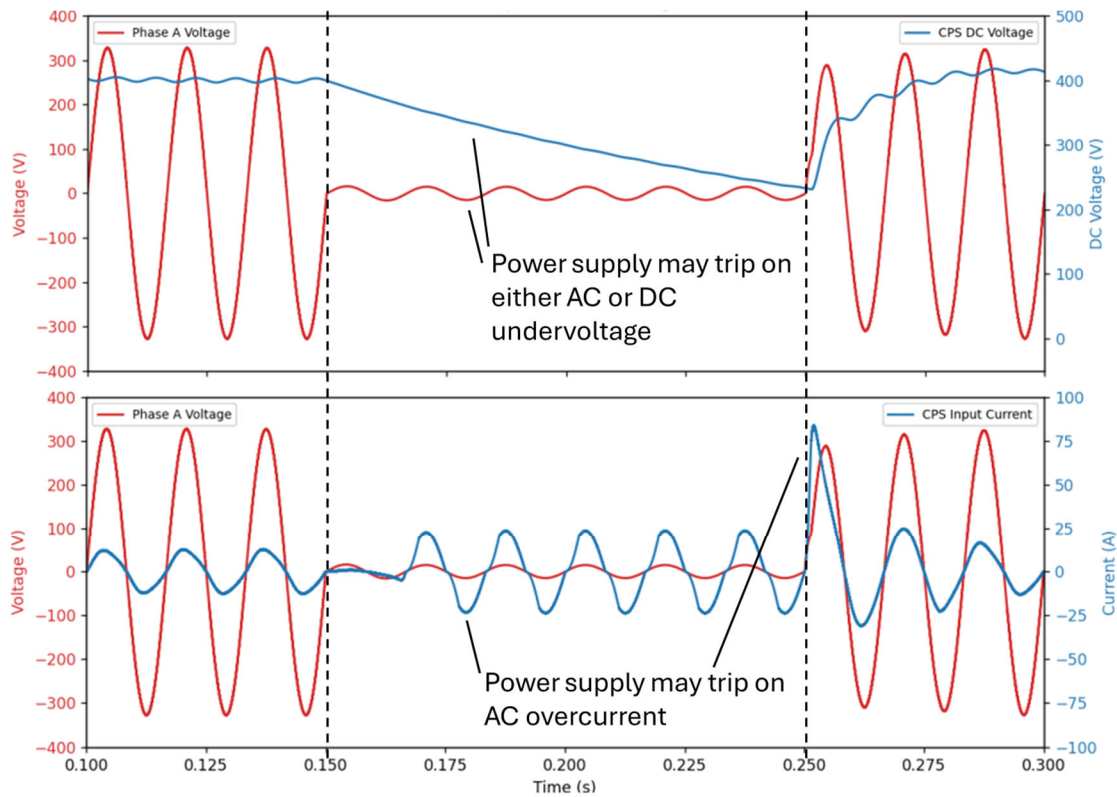


Figure 26: Example Response of PFC Converter (Called the “CPS” in the Figure Legend) to Severe AC Voltage Sag [72]. Annotations Indicate Features Which May Cause Protection Functions to Operate.

With rack-level energy storage becoming increasingly common for data centers (see designs 3—6 in Section 3.1), there are opportunities for this ride-through behavior to be improved without hardware changes. Rack-level storage can be used to supply energy to the DC link capacitor during AC voltage sags, eliminating the DC undervoltage and AC overcurrent.

3. Protections within UPS: If the ITE is protected by double-conversion UPS, the factors in (2) do not apply, and it is the protection settings of the UPS that control ITE ride-through. Modern UPS rectifiers invariably possess AC current limiting control, and the battery converter is designed to provide additional energy to support the DC link voltage when the rectifier is in its current limiting mode. For many excursions in grid voltage, the UPS battery can adequately regulate the DC link voltage and prevent any adverse impact to the downstream load.

Figure 27 illustrates the simulated response of a double-conversion UPS riding through a severe three-phase fault occurring at $t = 2$ s and cleared at $t = 2.1$ s. In response to the voltage sag, the input current increases in an attempt to maintain a constant DC link voltage (and, as a result, a constant input power), but the current limit is rapidly reached. The battery output current rapidly increases to provide the DC link voltage with additional support, and the resultant effects on the output current and voltage are negligible.

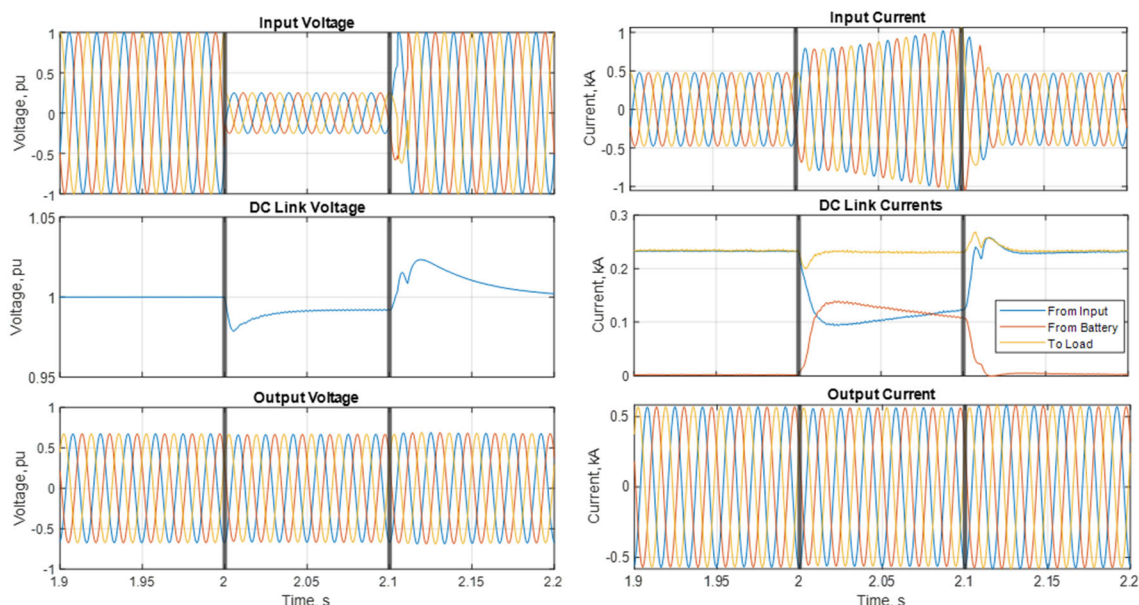


Figure 27: Simulated response of double-conversion UPS configured to ride-through a severe three-phase fault [72].

In reality, few UPS would ride through the fault illustrated in Figure 27. Because data center ride-through has become important only recently, most existing UPS protections are set conservatively (i.e., they trip quickly and for shallow voltage sags) so as to minimize the risk of damage or malfunction in either the UPS or downstream equipment. However, as data center owners have become more aware of ride-through impacts, UPS OEMs have been revisiting their stated ratings and developing new firmware features to permit a greater degree of ride through (i.e., they remain connected to the grid for more significant voltage excursions and for a longer period of time).

Ultimately, the low voltage ride through (LVRT) performance of the UPS is then determined by its ability to limit rectifier current during abnormal voltage conditions, maintain synchronism with the grid, and maintain tight regulation of the output inverter's AC voltage. OEMs specify LVRT limits for their UPS based on the performance of their controls in these respects, but more restrictive limits can (and often are) implemented in the UPS protection—these vary from site-to-site and may be set by users. If the UPS is operating in eco-mode/bypass prior to an LVRT event, the UPS must rapidly trip the bypass switch (likely on a sensitive AC undervoltage protection) and transfer the load to the rectifier, with the battery converter providing DC link voltage support as needed.

At the time of writing, technical restrictions and site practices surrounding the ride-through capabilities of cooling load have yet to converge to a clear trend. Because most data center electricity demand comes from ITE, existing efforts have prioritized improving the ride-through of ITE before devoting significant efforts to the cooling loads. Many motor drives can be configured to achieve good ride-through performance with the proper controls [73]. However, the drives themselves are only one component of the cooling system.

The cooling systems of large data centers are complex systems, with many motors, sensors, controllers, actuators, etc. coupled to the same mechanical process. If even one of these devices malfunctions in response to a voltage sag, the entire cooling process may malfunction. Thus, it is a common practice to restart the entire cooling system in response to voltage sags,

which requires the temporary disconnection of all cooling load. Depending on the thermal system's design and the data center's tolerance for risk, the entire site may need to be disconnected in order to ensure subsequent recovery activities are not disrupted by any additional grid disturbances. There are a wide variety of cooling system designs in use today [6], and data center cooling is the focus of intense research and development [74], primarily in response to the significant increases in heat density associated with near-future AI platforms.

Short-Time Demand Variations from AI Training and Inference

It is common for the power consumption of individual processors to vary quite rapidly on a millisecond timescale when performing intensive tasks. For most computing tasks, these variations tend to cancel one another out and the data center's site-level demand is quite smooth. In the case of parallel computing processes, however, the rapid variations in processor-level power consumption become correlated. As a result, the variations become significant at the site level. At the time of writing, this phenomenon is almost solely attributed to the training and inference processes of large AI models. Because much of AI training follows the same basic structure, AI training waveforms have a very distinct signature. Figure 28 illustrates an example active power consumption waveform for training a large AI model. Each of the indicated time periods correspond to a specific stage of the training process.

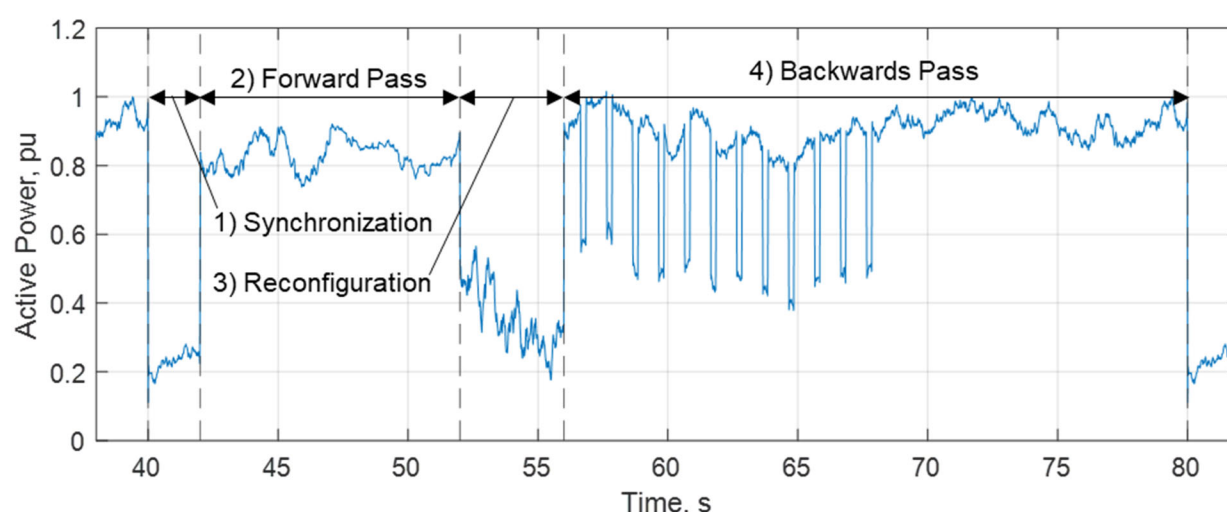


Figure 28: Exemplar Site-Level Active Power Consumption from AI Training Load, Annotations Demarcate Distinct Stages in the Training Process.

Generally speaking, the high power demand periods shown in Figure 28 correspond to computation-focused time periods whereas low-demand periods correspond to storage and communication-focused time periods. There are a variety of techniques for dispatching compute jobs to individual processors, but synchronous operation of site processors in this way is critical to obtaining good training performance [75] [76].

Many AI training iterations can be organized into the four stages shown in Figure 28:

- 1) Synchronization: Compute loads are inactive and ITE energy consumption is low—data transfers and synchronization processes are underway to prepare for the forward pass.
- 2) Forward propagation: Compute loads are active, and ITE energy consumption is high.

- 3) Loss function computation and reconfiguration: Some compute loads are active intermittently, power consumption tends to be moderate and choppy.
- 4) Backward propagation, parameter adjustment: high power consumption, rapidly drop off to low load afterwards.

Backward propagation usually takes roughly twice the time forward does [76] [25] [77]. The duration for a single round of training can vary widely but is on the scale of tens of seconds for a large model at a hyperscale facility.

The brief drops in consumption included in the first half of the reverse pass ($t = 56$ to 68 s in Figure 28) have been anecdotally observed in published waveforms [76] [25] [77] but may occur either at other times in the training process as well or not at all. These could depict a specific style of parallelization and indicate a time period where more frequent data exchange between individual processors is necessary.

5.1.4 Implications of DC Distribution

In section 3.1, we introduced three near-future data center concepts where the IT loads are supplied via a DC distribution, operating first at low voltage (e.g., 400 or 800 VDC) and then medium voltage (e.g., 20 kVDC). In all cases, there is a need for a high-power, three-phase AC/DC conversion stage interfaced with the grid. The application needs are similar to those of three-phase double conversion UPS, and a three-phase voltage source converter based on Si IGBTs or SiC MOSFETs is a likely candidate. Controls for such a converter could plausibly be designed to meet performance requirements such as those given in IEEE 2800 [19].

In the library's alpha release, data centers with DC distribution have been modeled much like UPS-based data centers—the UPS output inverter is replaced by a DC/DC converter which in turn serves IT load. To manage the technical scope of the DML's initial release, a basic buck-boost DC-DC converter is used (`DC_bi_avm`). Further representation of the DC system will require the development of additional models to represent LLC converters, high frequency transformers, and solid-state transformers.

Developing EMT models for these more realistic DC/DC step-down converter concepts should be a priority for follow-on EMT model development. Further consideration should also be given to neutral-point clamped (NPC) converter and multi-level modular converter (MMC) VSC, which are more practical for medium-voltage AC/DC conversion but introduce additional balancing controls. It is possible that the dynamics of these balancing controls will be unimportant for grid level studies, even during grid disturbances such as faults. However, further investigation is required to confirm this.

5.2 Climate Control Loads

Most of the energy consumed by IT loads is dissipated as heat, and thus a significant fraction of total data center electricity consumption (10 to 40%) can come from climate control loads. Variance in cooling load primarily comes from climate and the extent to which energy-efficient building design [78] is employed (e.g., computational fluid dynamics to optimize air flow, air-side economization, water-side economization, hot/cold aisle containment). In terms of electrical equipment, these are predominantly small- or medium-sized fans and pumps driven by induction motors. These are used to:

- Humidify or dehumidify incoming air.
- Pump chilled water for facility-level air conditioning (part of the compute rack air conditioning (CRAC)).
- Move air across air conditioning radiators.
- Circulate air in compute rooms (this is a major source, the compute rack air handling (CRAH)).
- Pump coolant for rack-level liquid cooling solutions.

Rack-level liquid cooling is primarily used when compute load largely consists of AI training hardware (e.g., the NVIDIA GB200 platform [79]) as it is made necessary by the hardware's exceptionally high power density. Fan cooling done at the device or rack level is usually powered via low-voltage DC and is, from the perspective of grid-level modeling, effectively part of the compute load.

Humidity control and its role in data center electricity and water consumption has declined significantly over time, as it was formerly commonly believed that low humidities introduced significant risks to electronic devices by increasing the likelihood of damage from electrostatic discharge (ESD) [6]. Today, relative humidities down to 8% are often accepted. Dehumidification is still necessary in humid climates—common air pollutants form corrosive compounds at relative humidities above 60%, and data center humidities are kept below this threshold, even if such air pollutants are thoroughly filtered out before entering the data center.

Local climate and the data center developer's energy efficiency philosophy are the two driving factors for cooling load energy consumption. Cooler climates require air conditioning units to run less often and permit the use of air economization methods which greatly reduce overall cooling load. Data center efficiency is usually summarized in terms of power usage effectiveness (PUE), which represents the total facility energy consumption divided by the energy consumed by IT equipment. Thus, a lower PUE is better and 1 is the lowest possible PUE. Notionally speaking, a data center in a warm, humid climate might operate at a PUE near 1.4 or 1.6 whereas a data center in a cool, temperate climate might operate at 1.2. There are not strictly enforced guidelines for how PUE is measured and reported—comparing PUE across different facilities as a measure of energy efficiency performance is often misleading.

Managing data hall air flow is a critical aspect of cooling system energy consumption; suboptimal designs result in hotspots which are resolved in the field by lowering overall cooling setpoints. Optimizing air flow requires rigid design standardization and the use of computational fluid dynamics (CFD) modeling [6], making it more suitable for large scale and/or vertically integrated sites, as opposed to sites with a variety of tenants and equipment that changes on a regular basis.

Most data center pump and building-level fan loads are three-phase induction motors driven by variable-frequency drives (VFDs) [6], as opposed to motors directly connected to grid power. VFDs are increasingly common, even in residential appliances, and they are particularly attractive for data center applications for their ability to improve overall cooling system reliability and efficiency due to the improved control they provide over motor speed. The prevalence of VFDs in data centers has important implications for power system modeling—the dynamics of

the cooling load will be primarily determined by the characteristics of the VFD's power electronic front end, rather than those of the induction motor and associated mechanical load.

Front-end power electronics for small (i.e., several HP or less) VFDs are usually either diode rectifiers or voltage-source converters (VSC), which respond very differently to grid disturbances. Diode rectifiers are much more common due to their lower cost and higher efficiency—the primary benefit of using a VSC over a diode rectifier for a VFD front end is the reduction in current harmonics and is, in some circumstances, a cost-effective option for complying with IEEE 519 harmonic limits [80] (most utilities require compliance with these limits as part of the interconnection agreement). Given the small size of the individual cooling loads in data centers, we assume that data center designers typically employ more common approaches for harmonic control (e.g., passive components such as shunt filters and series reactors), and the data center VFD models use diode rectifier front ends.

Scope of DML Components

The DML contains several components for representation of cooling loads. Both single- and three-phase rectifier models (`rect_3x_full_wave`, `rec_six_pulse`) are provided, with the drive inverter and induction motor represented using a simple resistance. Complete drive models are also available (`vfd_avm`, `vfd_swm`).

These models should be applied with caution when evaluating low-voltage ride through. There may be other site-level controls. Large data centers often use a centralized chilled water plant and large rooftop chillers, both of which require that many electrically-powered devices (valves, control circuits, motor drives, etc.) be coupled to the same mechanical process. Even if only one or two of the devices connected to the same mechanical processes malfunction or resets during a voltage sag, this can result in improper operation of the entire cooling system. Thus, undervoltage drop-outs with either manual or automatic restarts are commonly employed—even if it appears that the drive load itself can ride-through without disruption, there are numerous control circuits which, while impractical to explicitly represent in grid-level EMT studies, may nevertheless define the LVRT capability of climate control processes.

5.3 Site Support Load

Site support load encompasses any load that does not fall into the category of climate control or IT equipment load and is generally a small portion (<10%) of the total site load. In addition to lighting, this includes small appliances and electronics typical of an office space environment. For grid-level studies, the dynamics of site support loads are generally assumed to be negligible and they are modeled as constant impedance loads.

5.3.1 Balance of Plant

The balance of plant (BoP) equipment included in the library represents a minimum of the on-site distribution system necessary to study how the aggregated load devices will respond to grid disturbances. As seen in Section 3.1, this mostly consists of aggregate representation of power transformers and cables. The intent is to provide a reasonable representation of the series impedance between major elements in the plant and the grid up to a frequency of several hundred Hertz.

Scope of DML Components

The only new components for BoP modeling introduced by the DML are low-voltage cable models (`LV_cable_1PH`, `LV_cable_3PH`) intended to provide the user with a convenient tool for approximating aggregate LV cable impedance without needing to collect a large quantity of data for use in a cable constants routine.

5.3.2 Energy Storage Systems

Energy storage systems (ESS) are an essential part of most data centers. The traditional role of ESS has primarily been to support critical cooling and IT load during grid power outages for the short time (e.g., 10 minutes) necessary to bring backup generation online and gracefully transfer the load. However, as data centers grow in size, are subject to LVRT requirements, and serve massive parallel computing processes, the role of energy storage in data centers is rapidly expanding.

Most ESS being considered or installed in data centers are either battery ESS (BESS) or supercapacitor ESS (CESS), meaning that they generally operate using DC and require a power converter to connect to the grid (either DC/AC or DC/DC, depending on whether the grid uses AC or DC). For grid-scale applications, the primary advantages of supercapacitor technology over Lithium-ion battery technology are its low maintenance requirement and tolerance of repeated cycling [81]. Supercapacitors can generally be sized to provide energy for tens of seconds whereas lithium-ion battery systems can supply energy for several hours. Supercapacitor and battery (primarily lithium ion) technologies are current subjects of significant research and development effort and market investment, and the performance and economics of these solutions may evolve significantly in the coming years.

Figure 29 illustrates five commonly considered ESS products and the points in the data center architecture they may be integrated. A simplified version of the centralized UPS architecture has been used here for the purpose of illustration—the ESS connection points identified are present in the near future data center designs as well.

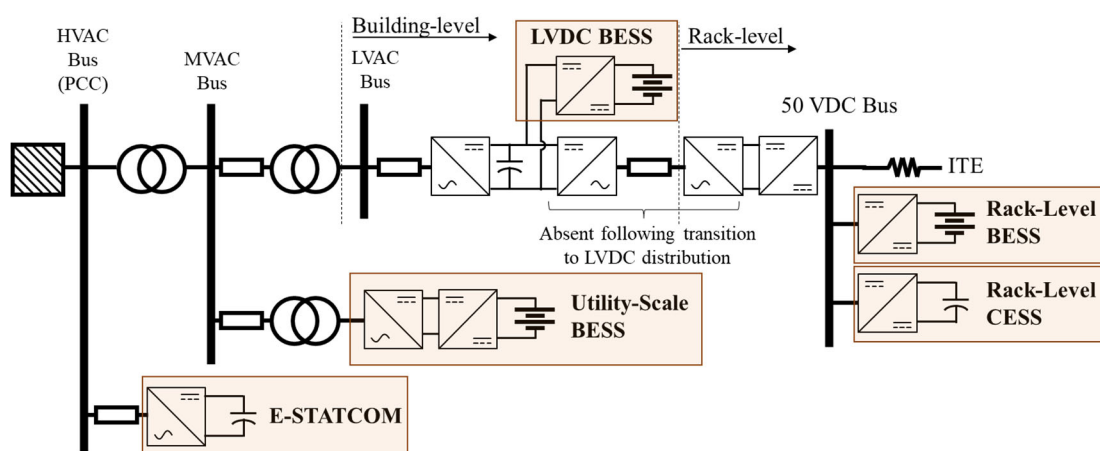


Figure 29: Five ESS Deployment Points for Modern and Near-Future Data Centers.

Both E-STATCOMs and utility-scale BESS have not traditionally been located with data centers but are currently marketed as near-term solutions for grid impacts from sudden variations in data center demand. An E-STATCOM is a relatively new kind of static synchronous

compensator (STATCOM). STATCOMs are large 3 PH inverters that do not have any load or generation connected to their DC link [82]. STATCOMs are used to provide dynamic reactive power support to enhance power system stability. An E-STATCOM differs from the traditional STATCOM in that it uses supercapacitors to obtain a very high DC link capacitance, allowing it to provide active power support as well, albeit for a short time period (e.g., 10s of seconds).

Differences in construction between E-STATCOMs and utility-scale BESS have important implications for the modeling of AI load smoothing applications. E-STATCOMs are often implemented using a single 3 PH inverter based on multi-level modular converter (MMC) technology [82]. This allows a single converter to achieve very high power (e.g., >100 MVA) and voltage (e.g., up to 750 kV) ratings. Utility-scale BESS, on the other hand, often use a large number of medium-power (e.g., 1 MVA), low-voltage (e.g., 480 VAC) 3 PH inverters [83]. As a result, the BESS requires a centralized plant controller which necessarily offers lower control bandwidth than the controls used for a single large inverter. Thus, E-STATCOM products can achieve significantly greater attenuation of active power oscillations than BESS (e.g., >95% vs. 70%) [82]. This is the result of the inverter architecture used, as opposed to any difference between supercapacitor and battery technology. The absence of an MMC-based BESS product in the market today is more likely the result of market forces, as opposed to a technical limit.

Both the E-STATCOM and utility-scale BESS seek to manage data center power fluctuations after they have already entered the AC power system. However, smoothing rapid power fluctuations is generally easier to accomplish in the DC portion of the system—there is no need to deal with frequency, phase, or reactive power, and simpler control approaches can be used. Site level power density, energy efficiency, and cost can all be improved by integrating the ESS more closely with the power electronics already existing in the data center. Near future data center design concepts seek to implement a mix of LVDC BESS, rack-level BESS, and CESS [11] [10]. These approaches may replace AC-interfaced solutions in the near future.

The LVDC BESS, as depicted in Figure 29, could correspond either to the BESS that have long been used in double-conversion UPS or a standalone device used as part of a future data center with a DC distribution system. The DC bus it connects to could either be internal to a double-conversion UPS or part of an LVDC distribution system. From a modeling perspective, the essential design feature is that the BESS is integrated at the LVDC level through a DC-DC converter with an output voltage of several hundred volts DC.

The LVDC BESS used in UPS today have two important limitations which can drive the need for an E-STATCOM or utility-scale BESS even at sites where there is significant UPS capacity installed:

1. UPS batteries are often sized to supply energy for tens of minutes. Batteries of this size will quickly wear out their useful life if used for continuous load smoothing.
2. The UPS rectifier may need to trip offline during a grid disturbance in order to ensure the disturbance does not impact the protected load. The critical implication here is that the ITE cannot remain connected to the grid in this case and a utility-scale BESS or E-STATCOM may be necessary in order to meet ride-through requirements

Rack-level BESS are primarily used to provide UPS functionality in distributed UPS architectures—in such designs there is no double-conversion UPS and thus battery backup must be implemented directly at the 50 VDC level. Within the Open Rack project, rack-level BESS are known as battery backup units (BBU) [84].

Rack-level CESS are used to provide demand smoothing at the rack level—rack-level BESS are sized to supply load for only several minutes and, like the LVDC BESS, will quickly age if used for load smoothing. Rack-level CESS are newly arrived to market and Open Rack specifications for their performance are not yet released.

Scope of DML Components

In the initial release of the DML, limited functionality is provided for representation of ESS that are not specific to data centers (E-STATCOMs or utility-scale ESS), but the power conversion technologies involved are similar enough to data center electronics that some representation is possible.

Built-in PSCAD components for batteries or capacitors may be used for the energy storage elements themselves. Alternatively, because battery state of charge (SOC) does not generally vary significantly during the time period of an EMT simulation, a DC voltage source and resistance may be used to represent the battery.

The AC/DC converter used in utility scale BESS can be represented using the `inv_gfm_droop_avm` component, which will naturally provide some level of oscillation suppression depending on the control gains and grid impedances used. That said, the model does not include functions specific to oscillation suppression or for replacing the active power consumption of site load that tripped in response to a grid disturbance.

The DML does not include models for controls specific to E-STATCOMs.

The DC/DC converter used in LVDC ESS, rack-level BESS, and rack-level CESS may be represented using the `DC_bi_AVM` component.

5.4 On-Site Generation

Many large data centers have a significant generation capacity on site. Traditionally, this has largely consisted of synchronous generators driven by reciprocating internal combustion engines burning diesel fuel. These have been used almost exclusively to provide a backup power source to the data center in the event of an extended utility outage. Such installations are generally not represented in grid-level studies, as a series of interlocks ensure the backup generation is never electrically connected to the grid. However, the variety of use cases and drives for on-site generation at data centers has expanded and now includes numerous scenarios where there is value in their representation for plant- or grid-level studies. Because this is an evolving and emerging topic, background is given on some of the drivers and challenges for co-located data center generation. While many of these factors are not explicitly related to EMT modeling, they significantly determine the engineering objectives and constraints that define the useful scope of EMT analysis.

Broadly speaking, there are three emerging use cases for on-site generation:

1. **Bridging power:** a data center wishes to commence operation for part (or even all) of its facility before utility power is available.
2. **Flexible operation to support grid reliability:** as a condition for receiving service, a data center operator must be able to reduce its net power consumption from the grid when instructed by grid operators. The data center operator wishes to do so without

curtailing any of their on-site processes, and so plans to use on-site generation to reduce their net consumption.

3. **Compliance with grid performance requirements:** as a condition for receiving service, the data center operator must condition their power waveform (e.g., reduce rapid fluctuations) or response to grid disturbances (e.g., improve low-voltage ride through).

Note that, while some grids offer markets and economic incentives pertaining to (2) and (3), the top priority for many data center developers remains the rapid procurement of sufficient energy supply. Thus, the primary justification for installing on-site generation capabilities beyond those necessary for emergency backup is to accelerate the data center's access to electricity.

It is worth noting that, for hyperscale facilities dedicated to AI model training, the additional uptime provided by installing emergency backup generation (typically a few hours a year if the facility receives service directly from the transmission provider) is often unnecessary. Thus, such facilities usually procure generation primarily to meet shortfalls in utility capacity or performance requirements.

The relevance of these use cases for a particular data center will significantly influence the kind of on-site generation employed (and consequently its representation in an EMT model), as well as the generation resource's potential relevance for EMT studies. A critical factor is whether the generation will support grid-connected operation. In such a case, the generation plant plays a central role in grid-level EMT studies. However, there can be compelling reasons to deploy generation solely for islanded operation. In such a case, the generation plant may need very little representation in grid-connected studies, but EMT analysis can still play a useful role in plant-level design studies, particularly with respect to the generation facility's ability to meet dynamic performance criteria (e.g., voltage and frequency regulation) during various plant operations.

For both (1) and (2), it is sometimes possible to deploy on-site generation without ever connecting the generation to the grid, which can simplify the overall interconnection process. Grid-connected generation must go through its own interconnection process and may be subject to its own set of performance requirements such as those in IEEE 1547 (for small generation facilities), IEEE 2800 (for transmission-connected IBRs), or NERC reliability standards (for generation capacities of 75 MW or more). These requirements are often applied at the facility level, and thus may result in stricter performance standards for the data center power system as well (e.g., lower permissible limits for harmonic emissions). Thus, there generally must be a strong justification for undertaking the extra cost and effort associated with making on-site generation suitable for grid-connected operation.

For example, the data center owner who purchases the generation plant may have difficulty recovering the generation plant's capital costs (either via sale of the plant or via revenue from electricity sales) unless the plant can be dispatched to sell electricity to loads other than the data center without significant modifications. Additionally, electromechanical generation is likely to have greater difficulty achieving stable and reliable operation when serving rapidly fluctuating AI training loads in islanded configuration¹. Thus, in applications where data centers are satisfied with the availability (i.e., uptime) of the local transmission system, it may be advantageous to have a utility-scale generation facility that is located nearby electrically but

¹ That is, islanded from the grid but still connected to the data center. All generators must temporarily be operated in an islanded condition as a part of startup.

designed and operated in a manner similar to typical utility-scale generation. In the long term, this may also allow the generation plant to transition to a more typical generation owner business model, simplifying operations for the parties involved and easing recuperation of the generation plant's capital cost via electricity sales. However, this approach requires the transmission system be eventually upgraded to facilitate the generation interconnection even if the data center is out-of-service. This may not be cost effective from a transmission system perspective and may require interim operating restrictions or remedial action schemes (RAS) which introduce their own costs and reliability risks. Thus, the viability of deploying co-located generation at a data center is likely to vary significantly by location and close coordination with local transmission planners is essential to ensuring that the plant has a feasible long-term path by which its capital costs may be recovered.

5.4.1 Characteristics of Small Standby Generation

The dynamics, characteristics, and modeling of utility-scale generation for grid-level studies is an enormous topic and beyond the scope of this report. Instead, this section focuses on small (e.g., <25 MW) generation units typically used for standby power. Such generators exhibit significantly different dynamics than the utility-scale generation, and this fact is a chief motivation for this section and their inclusion in the DML. In this discussion, we will focus on reciprocating internal combustion engines, as they have historically received little attention in the context of grid-scale modeling.

Other desirable generation technologies for standby power include generally popular technologies such as natural gas turbines, combined-cycle natural gas (for very large sites, e.g., over 500 MW) as well as solar photovoltaic (PV) or wind energy paired with battery energy storage. Less mature technologies such as small modular reactors (SMR) and fuel cells are also actively being procured for hyperscale data center projects [85] [86]. SMR technology uses a steam turbine and synchronous generator, whereas fuel cells require a DC/AC power converter. Further work is needed to understand the best practices for modeling these new generation plants in EMT studies (and perhaps in phasor studies as well). However, this is beyond the current scope of this report.

5.4.1.1 Reciprocating Internal Combustion Engines

Reciprocating internal combustion engines are conventionally used for emergency backup power and, in such cases, usually burn diesel fuel. The widespread availability, shorter lead times, and ease of transport of reciprocating engines has also made them an attractive means of meeting generation shortfalls for data center developers working on aggressive timelines. That said, engines burning diesel fuel require additional environmental permitting [87] and their permissible annual runtime is restricted (e.g., to 100 hours annually) in order to mitigate impacts to air quality. This is particularly troublesome for the tenant-based data centers as these hours of backup may be guaranteed to their tenants as part of a reliability agreement, meaning that they may not be able to meet the additional obligations related to grid support or bridging power. For these reasons, data center developers are increasingly looking to reciprocating engines burning gas or natural gas, which can be run much more frequently.

Historically, the ability of gas and natural gas engines to accept large changes in load without stalling has been significantly lesser than diesel engines. However, recent advances in engine design now allow these engines to meet the most stringent of industry standard load acceptance performance categories [88]. ISO 8528-5 defines transient performance specifications for reciprocating engine generators [89].

Table 10: ISO 8528-5 allowable frequency and voltage deviations in response to load steps [90].

Performance metric	Class G1	Class G2	Class G3
Maximum transient frequency deviation (%) for sudden power increase	≤ -15	≤ -10	≤ -7
Maximum transient frequency deviation (%) for sudden power decrease	≤ 18	≤ 12	≤ 10
Frequency recovery time (seconds)	≤ 10	≤ 5	≤ 3
Maximum transient voltage deviation (%) for sudden power increase	≤ -25	≤ -20	≤ -15
Maximum transient voltage deviation (%) for sudden power decrease	≤ 35	≤ 25	≤ 20
Voltage recovery time (seconds)	≤ 10	≤ 6	≤ 4

In addition to the three classes defined in Table 10, Class G4 indicates custom requirements based on an agreement between the customer and supplier. For applications with more sensitive electrical loads (such as data centers), it is common to use engines with Class G3 performance or some stricter set of requirements (i.e., Class G4) [88]. The percentage step change in load to which the requirements in Table 10 varies by engine, based on its braking mean effective pressure (BMEP). The first load step applied for many engines is usually somewhere in the range of 20 to 35% of rated engine power, but engines for standby applications advertise the capability to accept 100% of rated load in a single step [91] [92].

The load acceptance capabilities defined in ISO 8528-5 do not translate directly for data center applications; ISO 8528-5 testing is done using resistive load banks (a constant impedance load with respect to voltage) whereas the majority of data center loads are constant power (with respect to both frequency and voltage). This distinction is critical as excitation systems of standby generators often rely on Voltz/Hz control to meet performance requirements. This control varies output voltage in response to frequency variations, with the effect of improving frequency regulation but only insofar as the load's active power consumption is sensitive to changes in voltage.

Volts/Hz control is ineffective at improving frequency regulation when the generator is serving constant power loads, and so the effective load acceptance capability for data center applications can be significantly less than that indicated by ISO 8528-5 [93]. This has significant implications for grid code requirements related to LVRT and postfault active power recovery—most UPS and rack-level power supplies do not currently have a mechanism for detecting whether they are reconnecting to the grid or to backup generation. Consequently, they must use a slow ramp rate (much slower than that required by some emerging grid codes) to ensure they do not stall the engines when restarting on backup power. This could be addressed by varying the set ramp rate based on a control signal indicating whether the data center is connected to the grid. Another option is to add a frequency droop to the UPS or power supply active power controls, which would serve a role similar to the generator Volts/Hz control without delaying ramping when reconnecting to a high inertia system. This approach could lower installation

costs, but the frequency measurement method will require careful design to ensure an appropriate response during transients such as faults.

5.4.1.2 Suitability for Emerging Data Center Applications

As discussed previously, grid-connected operation of co-located generation resources introduces significant complexity but may be necessary for economic reasons. Additionally, with increasing transmission system congestion, there has been interest from grid operators in repurposing existing back-up generation for grid-connected operation. However, the decision of whether to support grid-connected operation is fundamental to the generation plant design, and retrofit is generally not economical. In this section, technical challenges associated with grid-connected operation of co-located generation resources are discussed. Some of these challenges relate to performance requirements required for reliable operation in a grid-connected application whereas others are simply limitations of the technologies.

Most of the standby generation units typically employed for backup power at data center facilities were not originally designed with grid-tied operation in mind. For example, the first generator sets certified to meet IEEE 1547-2018 achieved their certification only in late 2023 [94]. Meeting certain safety-related requirements such as those related to islanding detection can be challenging for small synchronous generators to meet [95]. Even if a standby generator set supports parallel operation with other generators in a small island, it is generally necessary to revise the frequency and voltage regulation controls to achieve stable operation when grid-connected. The controls needed to meet dynamic performance requirements in both grid-connected and islanded operation can be far more complex than those typically used in standby generation.

Standby generators are often deployed at the building level and employ low-voltage generators (as opposed to medium voltage). They tend to have less inertia, lower exciter headroom, and to experience lower short-circuit ratios. These factors make it more challenging to remain stable and connected during grid faults throughout the conditions necessary to meet requirements such as NERC PRC-29 [20]. Thus, retrofitting existing standby generation for grid-connected operation is, at minimum, an extensive engineering effort involving major equipment changes. In some cases, it may be impossible to meet grid performance requirements without near-complete replacement of the generation plant.

Despite the plausible stability challenges, reciprocating engines do generally possess the ability to vary their active power output far more rapidly than most other forms of electromechanical generation. This makes them an attractive option for data centers looking to deploy generation in order to meet grid support requirements associated with flexible interconnections. This includes response to operator requests for curtailment as well as ancillary services such as fast frequency response.

Little data is available on the ability of reciprocating engines to serve rapidly fluctuating loads such as AI training loads. Some public data is available regarding the torsional properties of reciprocating engines [96] [97] [98]. This data suggests that reciprocating engines are likely to possess one or two shaft resonances in the subsynchronous range, and that the amplification of the resonances could be significantly lower than that associated with large turbines (e.g., an amplification of 5 as opposed to 40). However, none of this data is directly applicable to an engine-generator application. Moreover, the steady-state mechanical torque provided by a reciprocating engine often has non-negligible fluctuations in the subsynchronous range—this

constitutes another ongoing potential source of fatigue which could limit the engine's ability to tolerate additional torque ripple.

Scope of DML

On-site generation models, tailored for the three emerging use cases identified at the beginning of this section, have been introduced with the beta release of the DML:

`Gen_recip`: A reciprocating engine model including controls for islanded operation and basic grid-connected operation.

`Gen_sync`: An autosynchronizer device which can synchronize a generator's output voltage with the grid voltage prior to interconnection, allowing smooth connection to the grid.

These models are intended to support exploratory studies at both the grid and plant levels. With proper parameter selection, these models can provide some initial assessment of the suitability of different generation plant technologies and designs. As the variety and complexity of generation facilities at data centers is expected to grow rapidly in the near future, there will likely be a need for more sophisticated plant-level studies at the design stage.

6.0 Power System Models

In this section, simulation results obtained using the DML models and case files are presented to demonstrate the model's behavior and potential use cases. DML contains simulation files (.pscx format) which represent different power system models for simulations. The simulation files include the generic data center designs introduced in Section 2.0, as well as some benchmark cases useful for illustrating grid-data center interactions or testing out the more complicated models.

NOTE: The parameters used in these models (cable impedances, protection setpoints, controller gains, etc.) are intended to be reasonable and illustrative, but they are not based on comprehensive surveys and can vary significantly site-by-site. The provided parameters are meant to provide users with a functional and reasonable model, but may not be representative of typical parameters at real sites.

6.1 Inverter Model Demonstration (DML_Inverter_Demo)

The DML_Inverter_Demo model (Figure 30) is a simple test system for 3 PH inverter models such as `inv_gfl` and `inv_gfm_droop_avm`. It contains two copies of the same basic transmission system (a) in order to facilitate convenient comparison of any two 3PH inverter models (b). For 3 PH inverters that perform DC voltage regulation, the DC side should be modeled as a current source (c)—otherwise, a voltage source should be used. The DC current source model includes a basic momentary cessation function (d), which is necessary to avoid DC voltage instability during close-in faults.

Figure 31 illustrates the PCC voltage and current obtained for a line-to-line (L-L) transmission system fault using both `inv_gfm_droop_avm` and `inv_gfm_droop_swm`, illustrating the similarity of the two models' low frequency behavior.

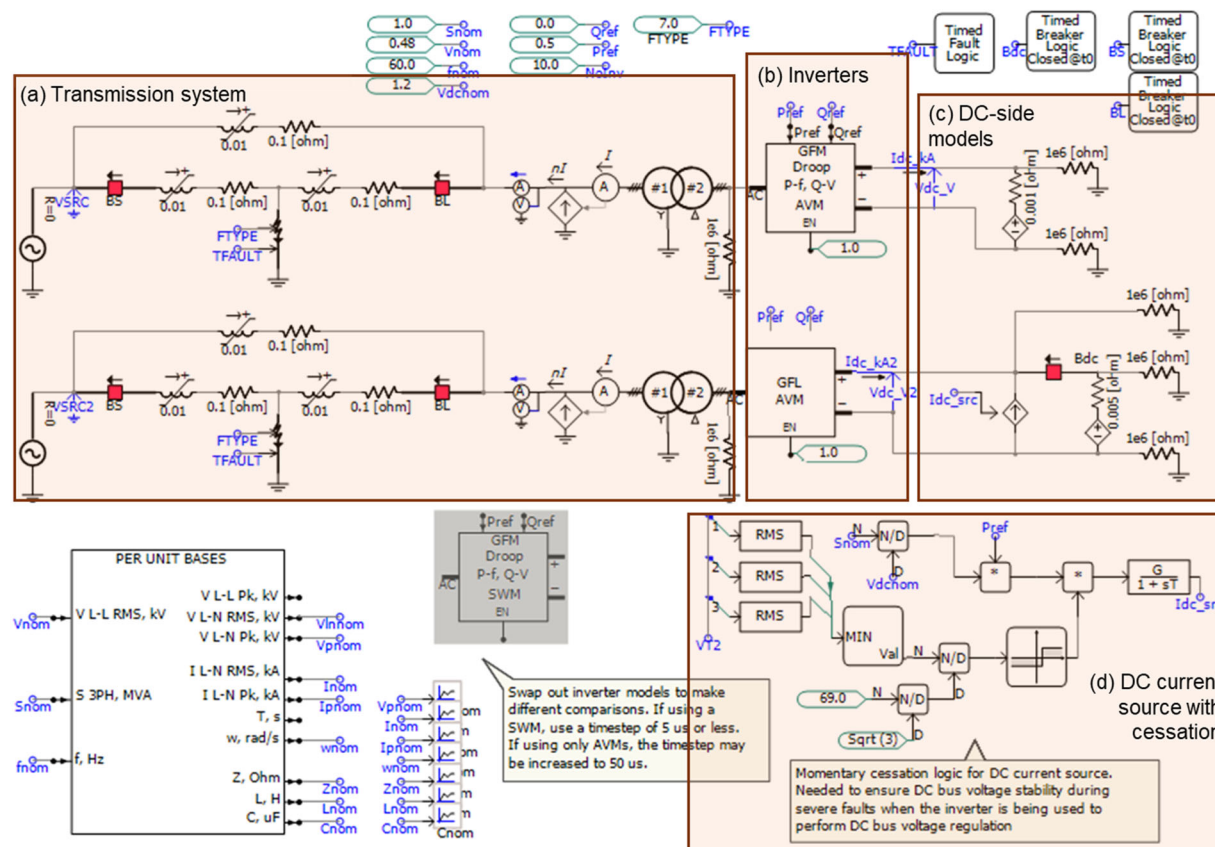


Figure 30: Overview of DML_Inverter_Demo Model.

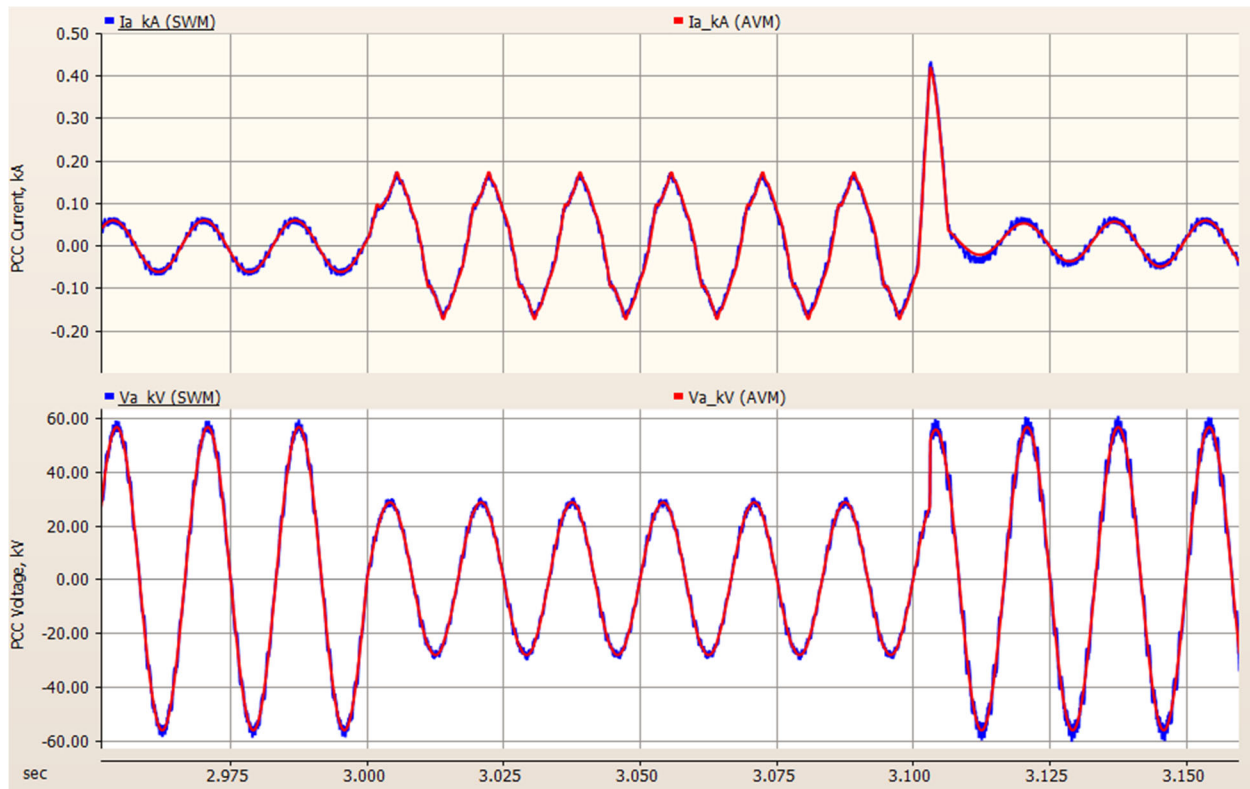


Figure 31: Comparison of L-L Fault Response from `inv_gfm_droop_avm` and `inv_gfm_droop_swm`.

6.2 DC-DC Converter Demonstration (DML_DC_DC_Demo)

The `DML_DC_DC_Demo` model (Figure 32) is a test system for DC-DC converter models, `DC_bi_avm` and `DC_bi_swm`. A timestep of 5 μ s should be used if the SWM is used. However, if the SWM is disabled, the model timestep can be increased to 50 μ s. The transmission system model is identical to that used in the `DML_Inverter_Demo` model.

Figure 33 compares the response of the SWM and AVM DC link voltage (top) and current (bottom) for a L-L transmission system fault. Observe that there are small but noticeable differences between the model. This is because the losses of the DC-DC converter, which are imperfectly approximated in an AVM, play a significant role in determining its transient response. This is in contrast with the case of the 3 PH inverter (refer back to Figure 31), wherein this differences in losses has a negligible influence on the inverter dynamics and the SWM and AVM are more or less identical for the purpose of grid-level studies.

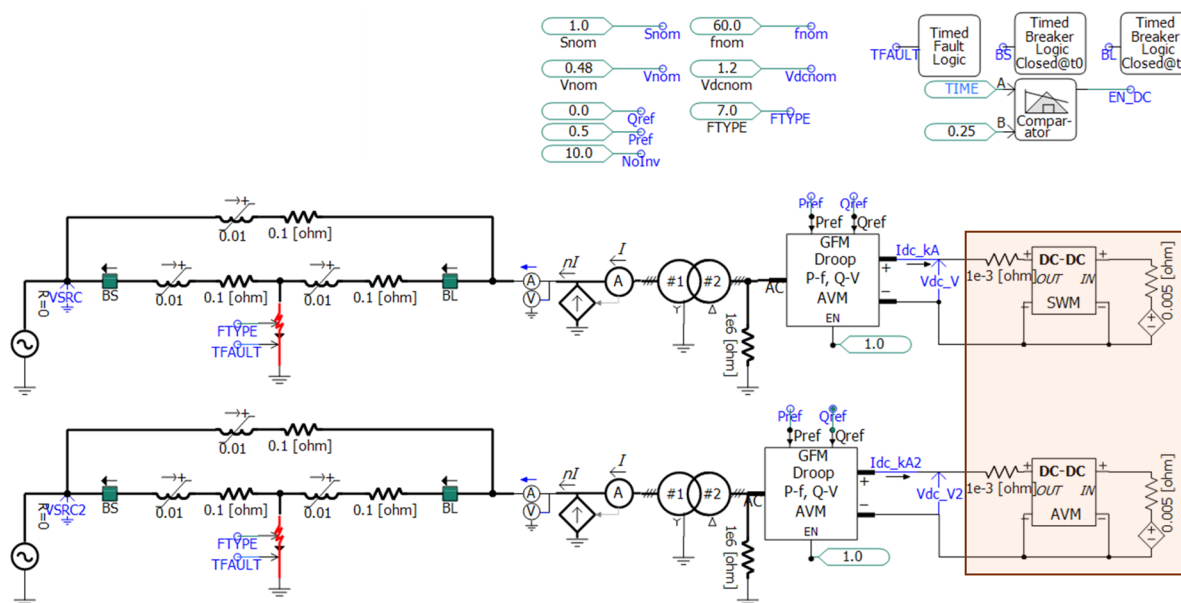


Figure 32: Overview of DML_DC_DC_Demo Model.

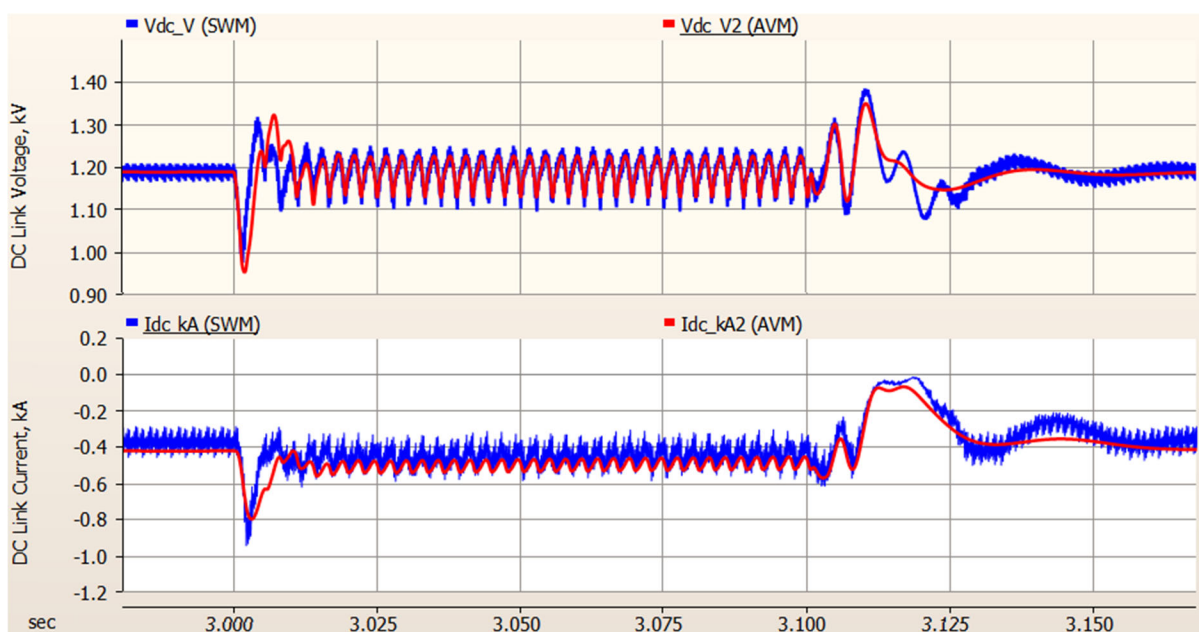


Figure 33: Comparison of SWM (Blue) and AVM (Red) Response to Transmission System L-L Fault.

6.3 PFC Converter Demonstration (DML_PFC_Demo)

The DML_PFC_Demo model (Figure 34) is a test system for PFC converter models, `pfc_avm` and `pfc_swm`. It can be used to compare the SWM and AVM or to evaluate different LVRT strategies for single-phase PFC converters. A timestep of $1 \mu\text{s}$ should be used if the SWM is used. However, if only AVMs are used disabled, the model timestep can be increased to $50 \mu\text{s}$. The transmission system model is identical to that used in the DML_Inverter_Demo model.

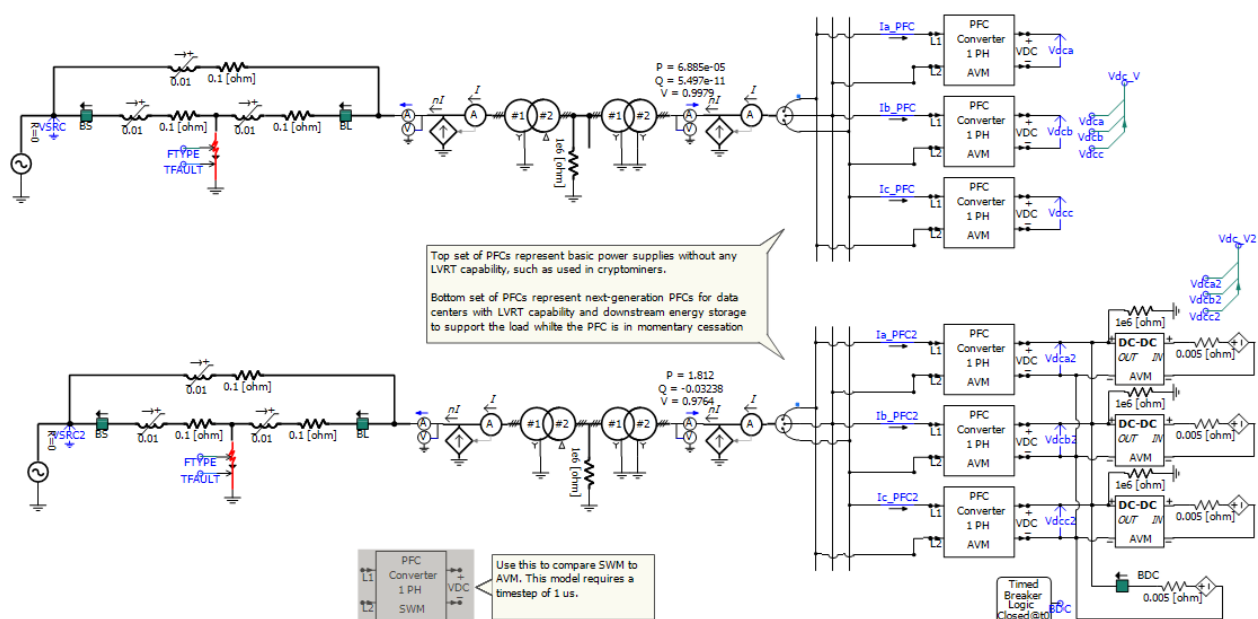


Figure 34: Overview of the DML_PFC_Demo Model.

Figure 35 compares the A PH current of the SWM to the AVM for a three phase fault at $t = 3$ s. At roughly $t = 3.11$ s, the PFC converter trips (due to a DC link overvoltage) and the current at the PCC drops to nearly zero. There is no visually apparent difference between the SWM and AVM, the two traces (red and blue) overlap closely.

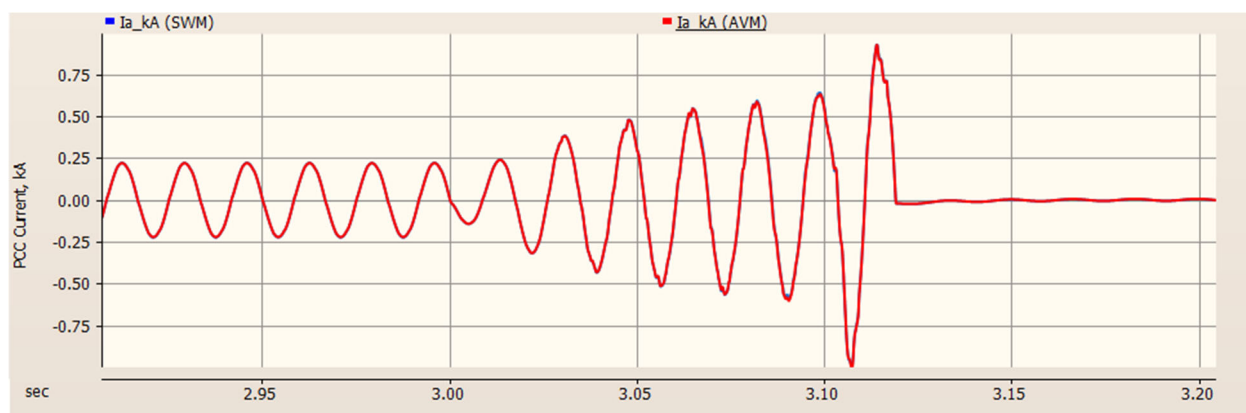

 Figure 35: Comparison of Fault Response of `pfc_avm` (Red) and `pfc_swm` (Blue) Fault Response.

Figure 36 compares the fault response of a PFC without (red) and with (blue) ESS and LVRT ride-through capabilities. The ESS is integrated via a DC-DC converter (`DC_bi_avm`) as shown in the bottom right hand corner of Figure 34. For this converter, momentary cessation is enabled. Without ESS and momentary cessation, the PFC converter draws significant current during the fault, and trips when the fault is cleared due to a DC link overvoltage. With momentary cessation, the power supply regulates its input current to approximately zero during the fault—the brief spike observed at $t = 3.10$ s is the result of the rapid voltage recovery following fault clearing. While not visible in Figure 36, the DC-DC converter supplies energy to the DC link while the PFC converter is in momentary cessation, allowing the load to continue functioning and providing a smooth transition back to grid power after the fault has cleared.

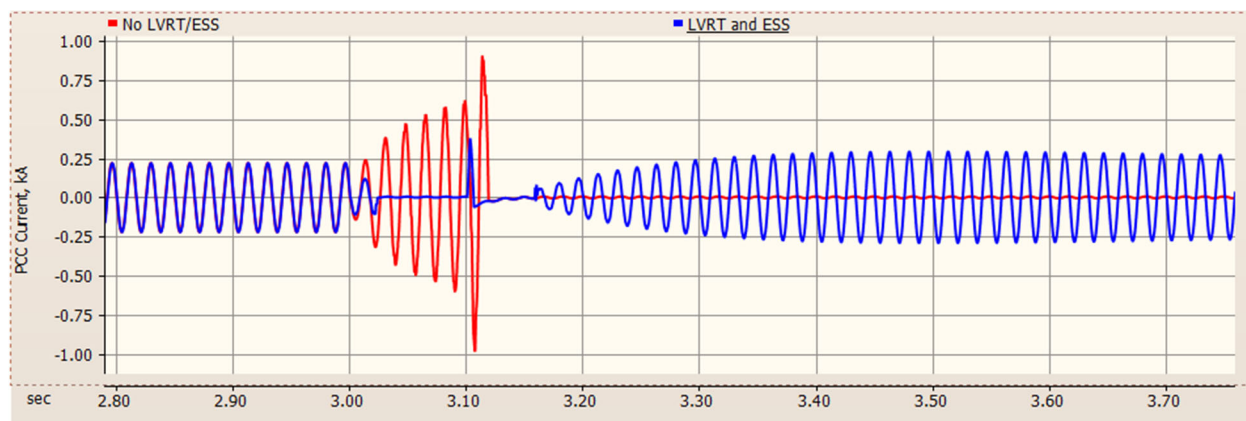


Figure 36: Comparison of Fault Response of PFC Without ESS to Provide LVRT (Red) and with (Blue).

6.4 Reciprocating Engine Demonstration (DML_Gen_Demo)

The DML_Gen_Demo system is a test system illustrating the functionality of the reciprocating engine genset model (`gen_recip`) and autosynchronizer (`gen_sync`) components. Figure 37 illustrates an overview of the test system.

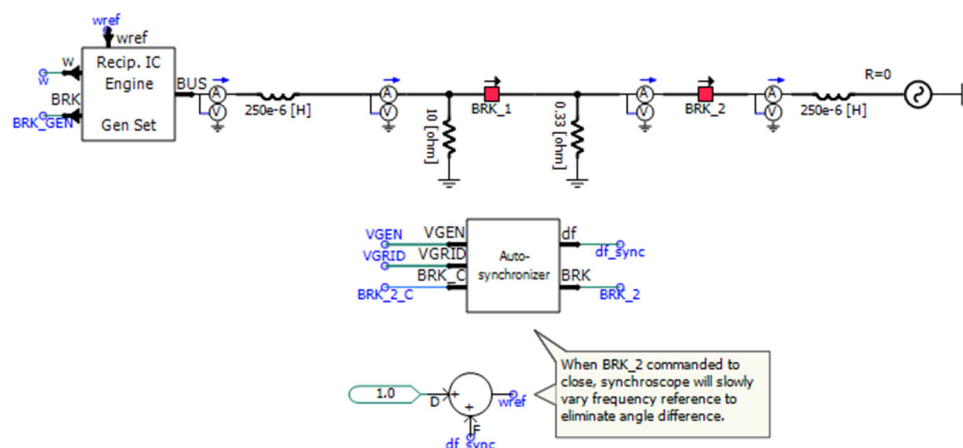


Figure 37: Overview of the DML_Gen_Demo model.

The simulation contains of two major events—load acceptance and grid synchronization. Load acceptance takes place at $t = 35$ s. BRK_1 is closed, connecting the 10 Ω resistor to the generator. Figure 38 illustrates the generator active and reactive power in response to the added load. The temporary drop in active and reactive power output immediately following the load is the result of the Volts/Hz control present in the exciter, which has reduced the generator's AC voltage output in order to reduce the active power output. This mitigates the speed reduction caused by the sudden load acceptance and the associated risk of engine stalling.

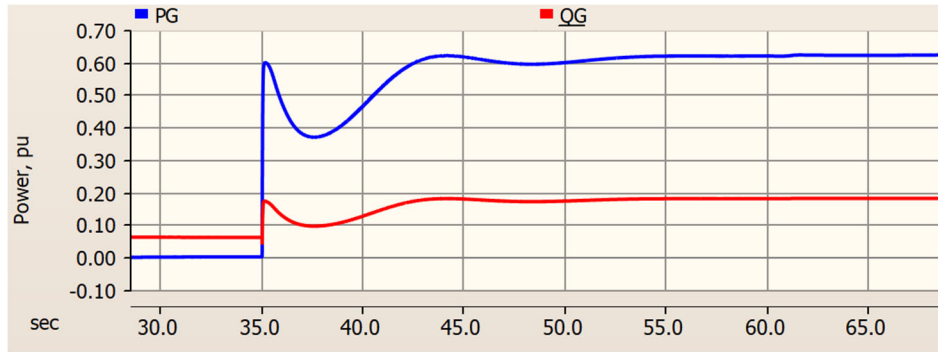


Figure 38: Response of generator active and reactive power output to load acceptance.

The autosynchronization event begins at $t = 60$ s, where a close command is sent to the `gen_sync` component controlling BRK_2. This component passes the received close command to the controlled breaker only when the voltages on either side of the breaker satisfy user-specified tolerances for magnitude, phase, and frequency. These are not satisfied initially and so breaker closing is delayed. The autosynchronizer adjusts auxiliary speed reference signal, “df_ref,” to vary the engine governor output and reduce the slip angle between the generator and grid voltages. This may be seen in the top plot of Figure 39, where the speed gradually increases from $t = 60$ s to $t = 95$ s. The small, persistent ripple in generator speed is the result of the unsteady mechanical torque created by the reciprocating engine.

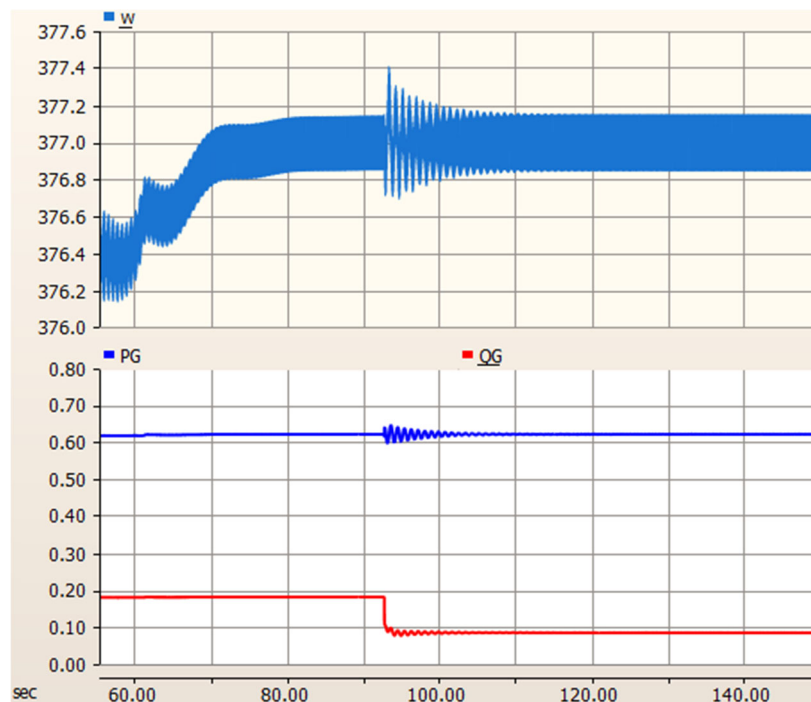


Figure 39: Response of generator angular speed (top) and power (bottom) to autosynchronization event.

At $t = 95$ s, the phase difference is within the tolerance allowed by the autosynchronizer and the breaker close operation is performed. A power swing still follows the breaker closing, but it is small in amplitude and unlikely to disrupt proper operation of the generator or grid. The reactive power supplied by the generator decreases as some of the reactive power consumed by the network’s series reactance is supplied by the grid.

6.5 Variable Frequency Drive Demonstration (DML_Drive_Demo)

The DML_Drive_Demo is a test system to demonstrate the variable frequency drive (VFD) cooling load models, including the switching model VFD_SWM and the average value model VFD_AVM. Figure 40 provides an overview of the test system.

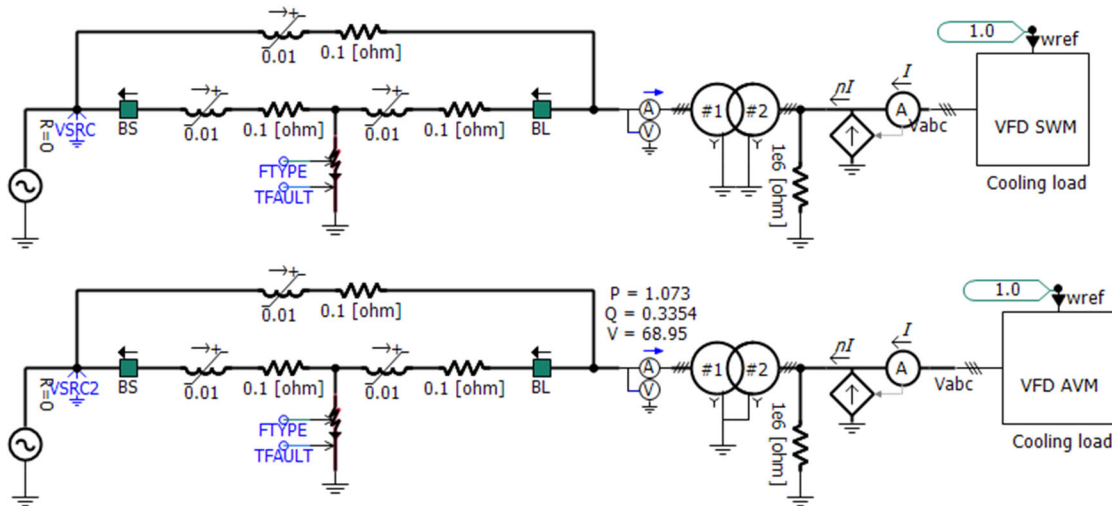


Figure 41: Overview of the DML_Drive_Demo Model.

To evaluate the dynamic behavior under grid disturbances, a three-phase voltage fault is applied at $t = 4$ s. Figure 42 and Figure 43 compare the active power and reactive power response using the switching model and the average model. As shown in the figures, both models operate at essentially the same steady state operating point. There is a slight difference between the active power, and the reactive power is nearly the same. When the fault occurs, the active power and reactive power both drop due to the terminal voltage drop. During voltage recovery, both models show a transient overshoot. This behavior is mainly caused by the DC-link recovery and induction machine dynamics under the open-loop V/Hz control. After the transient, both models settle back to their pre-fault active power and reactive power levels. Overall, the AVM closely matches the SWM in steady state and reproduces the main fault transient and recovery dynamics.

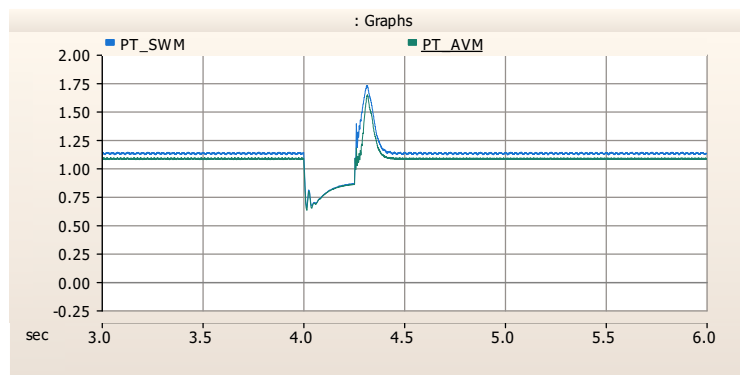


Figure 44: Active Power Response of VFD Models to 3 PH Fault.

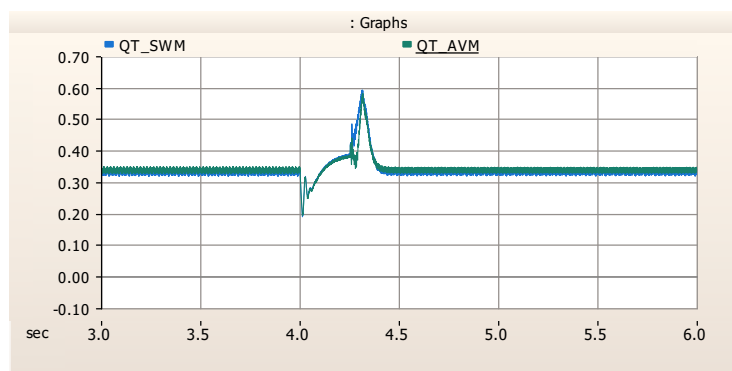


Figure 45: Reactive Power Response of VFD Models to 3 PH Fault.

6.6 PERC1 Model Comparison (DML_PERC1_Demo)

A simple 7-bus test system has been considered in this work to conduct a benchmarking test between the double-conversion UPS model used in the centralized UPS architecture (e.g., the DML_DC2_Central model) and the PERC1 model. PERC1 is being used by many utilities to represent data centers in stability studies. The test system used for this benchmarking has been presented in Figure 46 below.

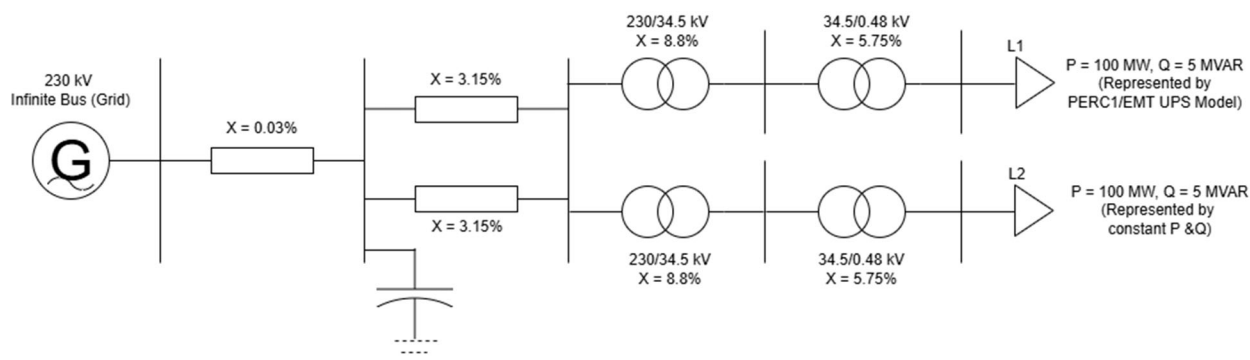


Figure 46: Test System Used for Benchmarking the EMT model with the Corresponding Phasor Model (PERC1).

Note that this is a benchmark of the double-conversion UPS model only—it is expected that the rack-level UPS and cooling loads can also be represented using PERC1, they require their own benchmarks and instances of PERC1. More comprehensive phasor benchmarking may be added in a future revision of DML.

The voltage sag waveform illustrated in Figure 47 is played into the infinite bus source for this test.

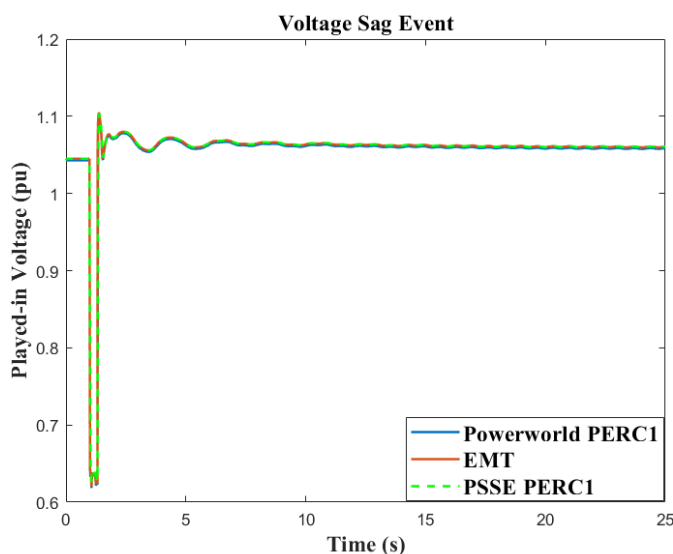


Figure 47: Played in Voltage Signal for the Voltage Sag Event.

The PERC1 model has been tested in both Powerworld and PSSE simulators. Powerworld simulations used software version v24 (build 577, patch date 2/18/2026). PSSE simulations used software version 36.5. The load 'L1' has been used to benchmark the datacenter UPS model. The load 'L2' has been represented by a simple constant-P and constant-Q type load. The PERC1 parameters used are as shown in Table 11.

Table 11: PERC1 Parameters Used for Comparison with EMT Model.

Parameter	Parameter Value	Parameter	Parameter Value
<i>Lfm</i>	0.8	<i>Ipmax</i>	1
<i>Qpratio</i>	0	<i>Ipmin</i>	0
<i>Dbfl</i>	0	<i>Iqmax</i>	0
<i>Dbfh</i>	0	<i>Iqmin</i>	0
<i>Kdroop</i>	0	<i>Fcease</i>	1
<i>Kvp</i>	0	<i>Vcease</i>	0.7
<i>Tvp</i>	0	<i>Tcease</i>	0.02
<i>Kvq</i>	0	<i>Tdelay</i>	0
<i>Tvq</i>	0	<i>Vrecon</i>	0.95
<i>Tap</i>	0	<i>Trecon</i>	5
<i>Tbp</i>	0	<i>Tramp</i>	10
<i>Taq</i>	0	<i>Frecon</i>	1
<i>Tbq</i>	0	<i>Tt</i>	0.02
<i>np</i>	0	<i>Tv</i>	0.02
<i>nq</i>	2	<i>Tf</i>	0.02

Figure 48 and Figure 49 illustrate the active and reactive power consumed by the double conversion UPS/PERC1 model. The PERC1 model performance is identical in both PSSE and Powerworld. Also, in all three model responses, the active and reactive power responses show the load goes into momentary cessation for 5 secs (based on the given input parameter *Trecon* = 5) when the played-in voltage goes below the chosen *Vcease* = 0.7 value.

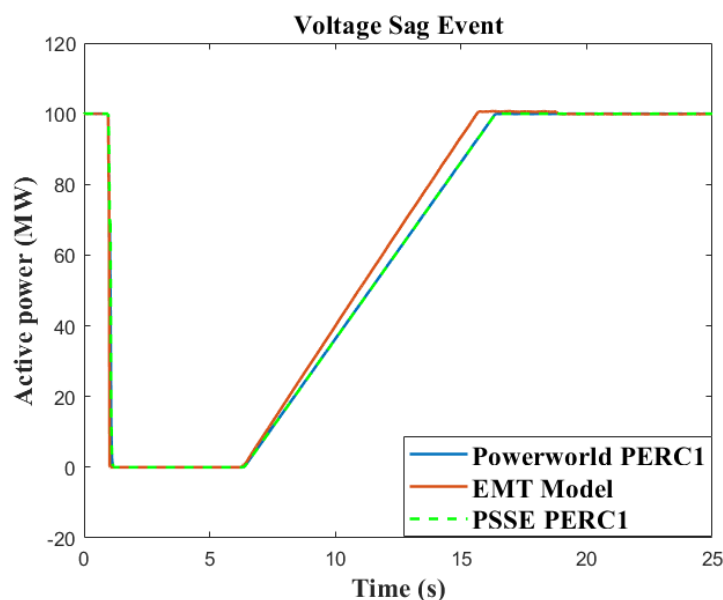


Figure 48: Active Power Comparison for Voltage Sag Event.

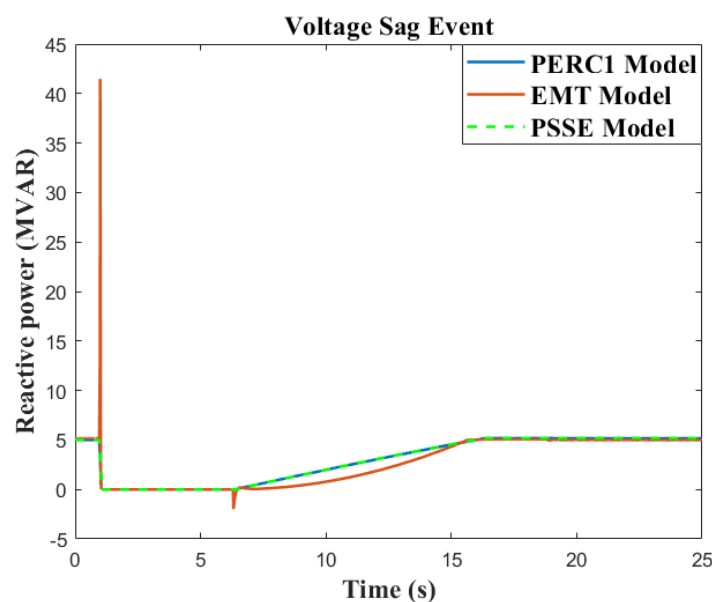


Figure 49: Reactive Power Comparison for Voltage Sag Event.

Slight differences in the transient response of the EMT and phasor models are primarily the result of control loops and transitions in operating mode that are not explicitly represented in PERC1. For example, the brief spike in reactive power present at $t = 2$ s is the result of the sudden shift in voltage phase angle at the UPS input caused by the fault. However, the UPS PLL and current regulators can respond to this jump in less than a power system cycle, making it unlikely that this needs to be recreated in the phasor model. Small transients at $t = 7$ s and $t = 18$ s are the result of the UPS rectifier and battery converter changing control modes. During normal operation, the rectifier uses a PI controller to regulate the DC link voltage. However, during momentary cessation and ramping, the battery converter performs this role.

The EMT model and PERC1 take different interpretations of the post-disturbance active power recovery function, and it is not yet apparent which better corresponds to real hardware. To

obtain a similar response for the two models, the *Tramp* parameter is chosen to be 12.5 secs in the EMT model and 10 s in the PERC1 model. This is because the UPS ramp-rate limiting operates by ramping its current limits from 0 to nominal over the specified time duration. Thus, when the UPS is only at part load, the time required to return to the pre-disturbance power consumption is lower. PERC1, on the other hand, operates by ramping its active power consumption to the pre-disturbance active power consumption over the same time period (*Tramp*), irrespective of the per-unit loading level.

In PERC1, the difference between UPS rating and loading level is captured by the load factor (*Lfm*). To achieve a consistent ramp rate between the EMT model and PERC1, it is necessary to either multiply the PERC1 ramp rate by *Lfm* or divide the EMT model ramp rate by *Lfm*. In this example, the latter option is chosen. Simulation software developers and OEMs have been contacted so that either the EMT model or PERC1 can be amended to better reflect actual UPS behavior in the future.

Even with measures taken to make the ramp times equivalent, the EMT model returns to pre-disturbance active power slightly more quickly than the PERC1 model. This is because the rate-limiting in the EMT model is applied to the current references (there is no active power reference) whereas it is applied to active and reactive power directly in PERC1. This means that the ramp rate of the active and reactive power is sensitive to voltage magnitude in the EMT model whereas it is not in the PERC1 model. In the test system used, the voltage magnitude is approximately 1.06 pu and so the EMT model returns to pre-fault power consumption in roughly $1 / 1.06 = 94\%$ of the time that the phasor model takes. Further collaboration and testing with OEMs is required to determine which behavior is more realistic.

6.7 Complete Data center Models

Before proceeding to describe the different data center models, we begin by discussing the transmission system model which is common to all the complete data center models included in the library (Figure 50). This model is meant to allow users to conveniently exercise different aspects of a data center's dynamics, primarily by simulating transmission system faults. The model consists of an equivalent generator (a), transmission system (b), and controls for convenient setting of network parameters (c).

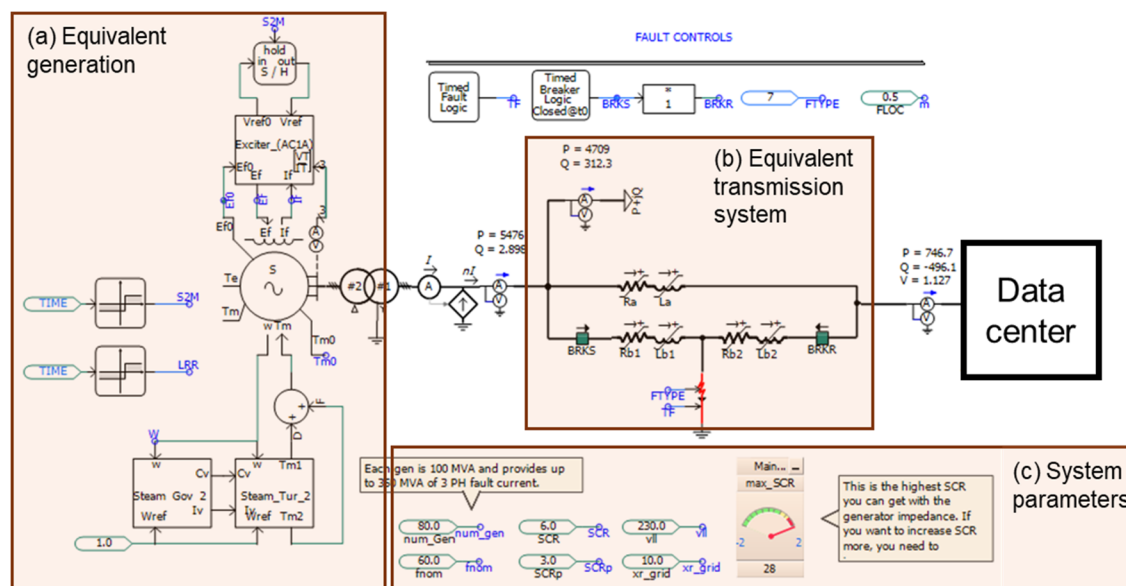


Figure 50: Transmission System Model Used for Complete Data Center Models.

The equivalent generator model uses a detailed synchronous machine model so that the effects of different data center ride-through and tripping behaviors on system frequency can be studied, as well as the ability of data center power electronics to maintain synchronism with the grid during weak grid conditions. Users should adjust the total generation by varying the value of “num_gen.” A value of num_gen = 1 results in a generator and generator step-up (GSU) transformer rated for 100 MVA that supplies 350 MVA of power to a bolted 3 PH fault on the high side of the GSU transformer.

The equivalent transmission system model allows for simulation of faults with varying electrical proximity to the data center while also capturing any potentially significant variation in short-circuit ratio (as defined based on the 3 PH fault current available at the data center PCC and rated capacity of the data center) that arises from fault clearing, which is implemented by opening the breakers labeled “BRKS” and “BRKR.”

Users define the data center short circuit ratio (SCR) when the breakers are closed using the constant labeled “SCR.” The SCR when the breakers are open is equal to “SCRp.” The value of SCRp must be lower than SCR—transmission system strength is always decreased by disconnecting lines, and violating this guidance will result in negative resistances and inductances that cause misleading simulation results. The “max_SCR” meter indicates the highest possible SCR obtainable based on the current value of num_gen and data center capacity. The values of SCR and SCRp must be lower than this value.

A fixed load component is connected at the high side of the GSU transformer (after the current scaling component) in order to simulate bulk system load on the equivalent generator. This is important as the loading of system generation will significantly alter the response of generator angle and frequency to faults and/or data center tripping. In the provided cases, the fixed load is configured to consist of 50% constant power load and 50% constant impedance load.

6.7.1 Simple Data Center (DML_DC1_Simple)

The DML_DC1_Simple model implements the Simple data center design introduced in Section 3.1 (Figure 51). The proper usage for the facility parameters (a) is described in Table 12. There are many additional parameters that can be configured via the parameters dialog for the individual components in the model. Documentation for component level input parameters can be found in Section 6.7.4. ITE is represented using the `pfc_avm` component (c).

IMPORTANT: PSCAD's built-in current scaling component does not support variable input signals. Thus, it is necessary to manually change the value of `No_pump_a`, `No_PFC_a`, and `No_fan_a` (located in (b) Current scaling values section of Figure 51) to match the values shown in the adjacent control panel. This inconvenience may be resolved in future versions by either introduction of a current scaling component that supports variables or improvements made to the PSCAD compiler.

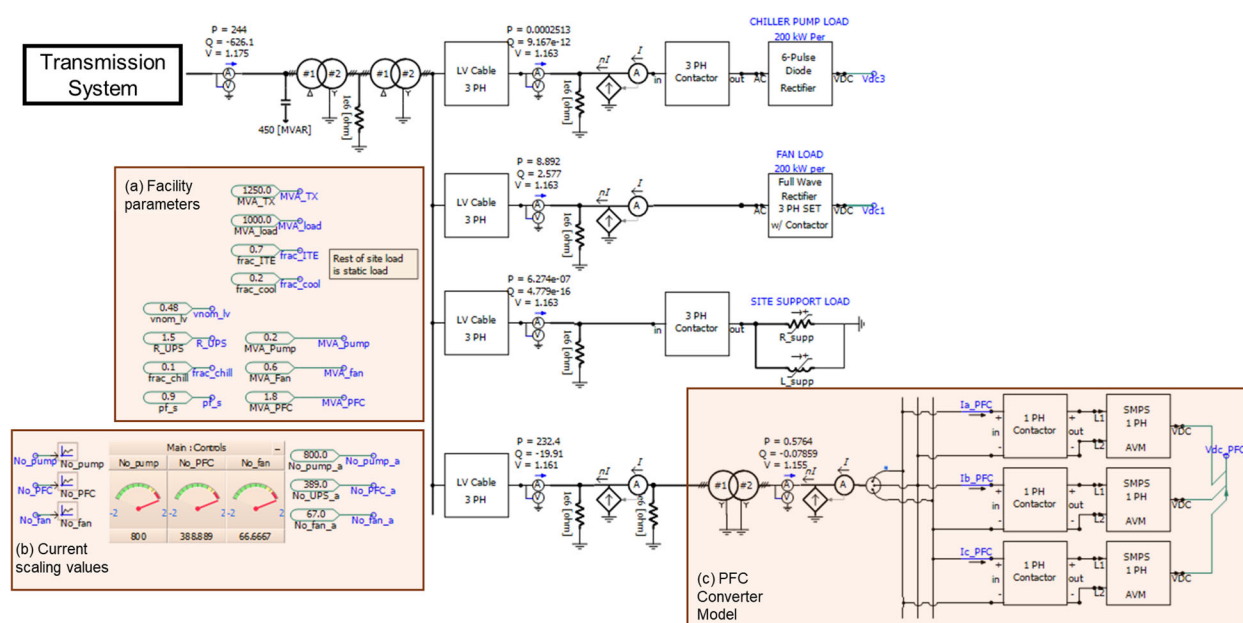


Figure 51: Overview of Simple Data Center Model.

Table 12: Facility Parameters for Simple Data Center.

Name	Units	Use
MVA_TX	MVA	In MVA solely because 3 PH transformer components don't support a variable rating, recommend setting to 1.2 to 1.5 times MVA_load.
MVA_load	MVA	Rated peak power consumption of the data center.
frac_ITE	N/A	Fraction (0 to 1) of peak power consumption allocated to ITE.
frac_cool	N/A	Fraction (0 to 1) of peak power consumption allocated to ITE. Whatever is not ITE or cooling load is assumed to be site support load and is modeled as a simple parallel RL circuit.
vnom_lv	kV	Nominal AC distribution voltage; recommended to leave at default value of 0.48 kV.
frac_chill	N/A	Fraction (0 to 1) of cooling load allocated to chillers (as opposed to fans).
pf_s	N/A	Power factor of site support load. Site support load is generally a small portion of total data center load and high precision for this value is unnecessary.
MVA_pump	MVA	MVA rating of individual pump model. Recommended to leave at default value of 0.2 MVA.
MVA_fan	MVA	MVA rating of individual fan model. Recommended to leave at default value of 0.6 MVA.
MVA_PFC	MVA	MVA rating of individual PFC converter model. Recommended to leave at default value of 1.8 MVA.

The kilowatt values for the fan and chiller pump loads are not tied to any specific hardware; these are simply the values for which the DC link capacitors have been sized. Current scaling components are used simply so that the user does not need to adjust passive components when adjusting the facility ratings.

6.7.2 Centralized UPS Data Center (DML_DC2_Central_UPS)

The DML_DC2_Central model implements the Centralized UPS data center design introduced Section 3.1 (Figure 52). The proper usage for the facility parameters (a) is described in Table 13. There are many additional parameters that can be configured via the parameters dialog for the individual components in the model. Documentation for component level input parameters can be found in Section 6.7.4.

ITE is primarily represented using a double-conversion UPS constructed out of the `inv_gfl`, `inv_gfm_droop_avm`, `dc_bi_avm`, and `ups_ctrl` components as described in Section 5.1.1. The load connected to the UPS output is represented using `load_ai_train`, which can also be used to represent a constant demand by letting the compute and resting load be equal.

IMPORTANT: PSCAD's built-in current scaling component does not support variable input signals. Thus, it is necessary to manually change the value of `No_pump_a`, `No_UPS_a`, and `No_fan_a` (located in (b) Current scaling values section of Figure 52) to match the values shown in the adjacent control panel. This inconvenience may be resolved in future versions by

either introduction of a current scaling component that supports variables or improvements made to the PSCAD compiler.

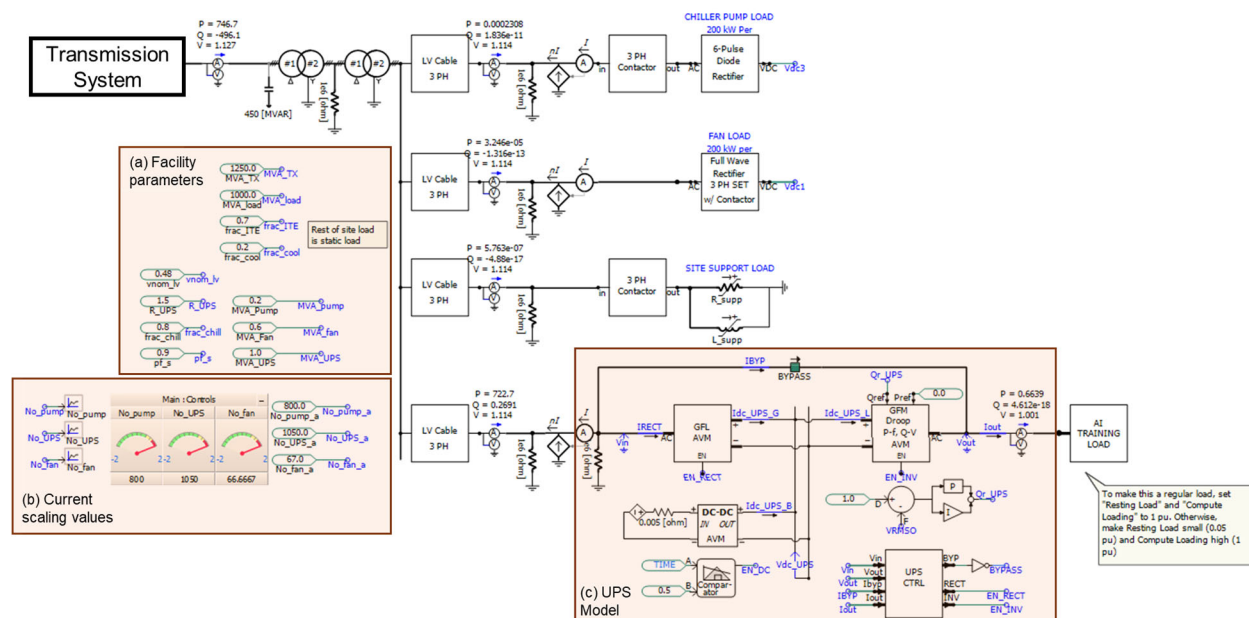


Figure 52: Overview of Data Center Model with Centralized UPS.

The proper usage for the facility parameters (a) is described in Table 13. There are many additional parameters that can be configured via the parameters dialog for the individual components in the model. Documentation for component level input parameters can be found in Section 6.7.4.

Table 13: Facility Parameters for Data Center with Centralized UPS.

Name	Units	Use
MVA_TX	MVA	In MVA solely because 3 PH transformer components don't support a variable rating, recommend setting to 1.2 to 1.5 times MVA_load.
MVA_load	MVA	Rated peak power consumption of the data center.
frac_ITE	N/A	Fraction (0 to 1) of peak power consumption allocated to ITE.
frac_cool	N/A	Fraction (0 to 1) of peak power consumption allocated to ITE. Whatever is not ITE or cooling load is assumed to be site support load and is modeled as a simple parallel RL circuit.
vnom_lv	kV	Nominal AC distribution voltage; recommended to leave at default value of 0.48 kV.
R_UPS	N/A	Sizing of UPS capacity relative to peak ITE demand. Usually varies from 1.2 to 2.0, depending on site reliability philosophy.
frac_chill	N/A	Fraction (0 to 1) of cooling load allocated to chillers (as opposed to fans).
pf_s	N/A	Power factor of site support load. Site support load is generally a small portion of total data center load and high precision for this value is unnecessary.
MVA_pump	MVA	MVA rating of individual pump model. Recommended to leave at default value of 0.2 MVA.
MVA_fan	MVA	MVA rating of individual fan model. Recommended to leave at default value of 0.6 MVA.
MVA_UPS	MVA	MVA rating of individual UPS model. Recommended to leave at default value of 1 MVA.

The kilowatt values for the fan and chiller pump loads are not tied to any specific hardware, these are simply the values for which the DC link capacitors have been sized. Current scaling components are used simply so that the user does not need to adjust passive components when adjusting the facility ratings.

6.7.3 Distributed UPS Data Center (DML_DC3_Dist_UPS)

The DML_DC3_Dist_UPS model implements the distributed UPS data center design introduced in Section 3.1 (Figure 3). The proper usage for the facility parameters (a) is described in Figure 53. There are many additional parameters that can be configured via the parameters dialog for the individual components in the model. Documentation for component level input parameters can be found in Section 6.7.4. ITE is represented using the `pfc_avm` component (c), which is configured to enter momentary cessation during voltage sags. Rack-level energy storage is represented using the `DC_bi_avm` component (d) and provides energy to the ITE DC link voltage when the PFC converter is in momentary cessation.

IMPORTANT: PSCAD's built-in current scaling component does not support variable input signals. Thus, it is necessary to manually change the value of `No_pump_a`, `No_PFC_a`, and `No_fan_a` (located in (b) Current scaling values section of Figure 53) to match the values shown in the adjacent control panel. This inconvenience may be resolved in future versions by either introduction of a current scaling component that supports variables or improvements made to the PSCAD compiler.

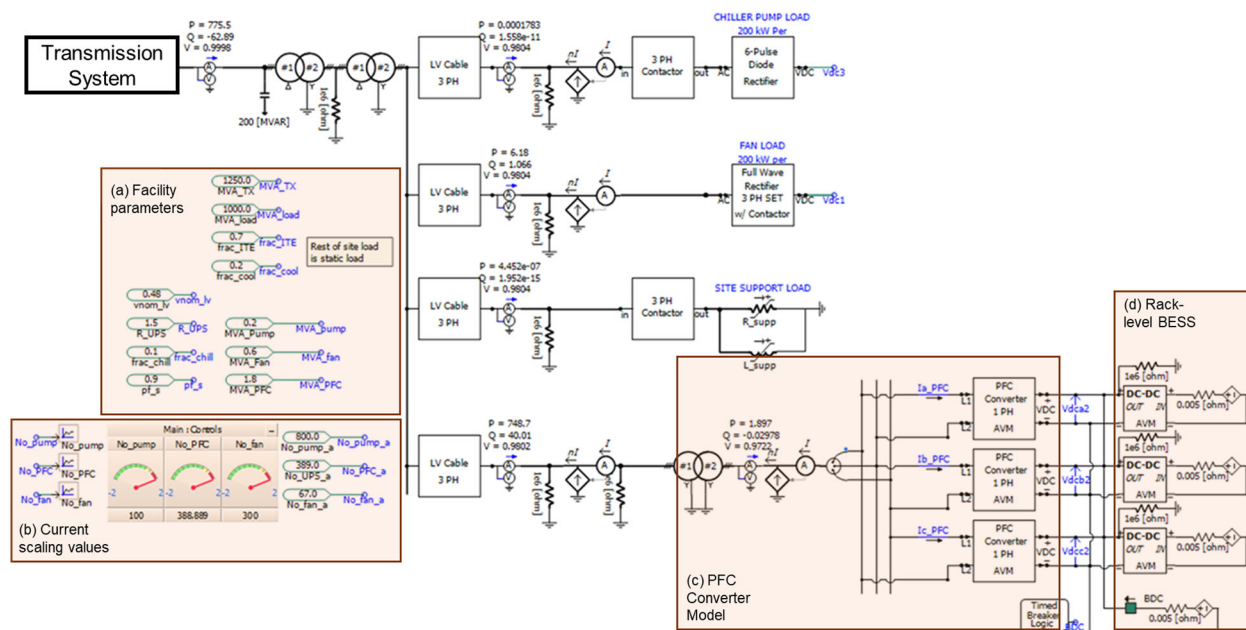


Figure 53: Overview of Data Center Model with Distributed UPS.

Table 14 lists the facility parameters for the distributed UPS data center.

Table 14: Facility Parameters for Distributed UPS Data Center.

Name	Units	Use
MVA_TX	MVA	In MVA solely because 3 PH transformer components don't support a variable rating, recommend setting to 1.2 to 1.5 times MVA_load.
MVA_load	MVA	Rated peak power consumption of the data center.
frac_ITE	N/A	Fraction (0 to 1) of peak power consumption allocated to ITE.
frac_cool	N/A	Fraction (0 to 1) of peak power consumption allocated to ITE. Whatever is not ITE or cooling load is assumed to be site support load and is modeled as a simple parallel RL circuit.
vnom_lv	kV	Nominal AC distribution voltage; recommended to leave at default value of 0.48 kV.
frac_chill	N/A	Fraction (0 to 1) of cooling load allocated to chillers (as opposed to fans).
pf_s	N/A	Power factor of site support load. Site support load is generally a small portion of total data center load and high precision for this value is unnecessary.
MVA_pump	MVA	MVA rating of individual pump model. Recommended to leave at default value of 0.2 MVA.
MVA_fan	MVA	MVA rating of individual fan model. Recommended to leave at default value of 0.6 MVA.
MVA_PFC	MVA	MVA rating of individual PFC converter model. Recommended to leave at default value of 1.8 MVA.

6.7.4 Mixed-Architecture Data Center (DML_DC4_Mixed)

The DML_DC4_Mixed model is a semi-aggregated data center model representing a complex facility that uses a mix of distributed and centralized UPS technologies, as well as on-site natural gas generation and a GFM BESS. This model is intended to provide an example of how the simpler data center models might need to be expanded to represent real-world facilities that contain a mix of different technologies. It also demonstrates the transfer of data center load to and from on-site generation, providing a basic example of the kinds of site operations which may become more common as data centers increasingly look to co-located generation to speed up the interconnection process.

This is not a real site design nor is it based on one. It is a purely fictitious scenario meant to illustrate non-homogeneities that can arise in practical situations and require a complex EMT model to represent. There are certainly opportunities to more fully utilize the generation and storage resources present in the model—the objective here is simply to provide a basic example of how these models can be used together, without needing to design advanced site-level controls.

Figure 54 illustrates an overview of the mixed-architecture data center. The site is rated for 1 GW consumption which has been built out in four major blocks, each which would consist of a number of large buildings in reality. The high-criticality ITE load uses double-conversion UPS

whereas the moderate-criticality ITE load uses rack-level battery backup. Blocks A through C are serving traditional data center applications with relatively constant active power demand, whereas Block D is being used to synchronous training of AI models.

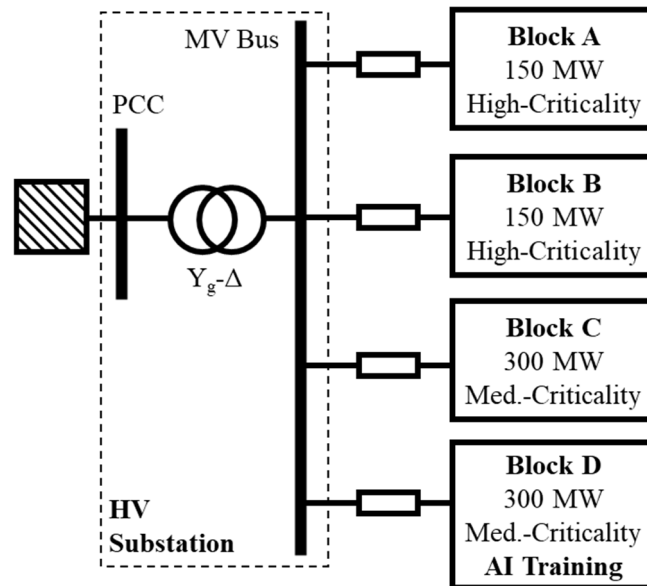


Figure 54: Single-line diagram of mixed-architecture data center.

Figure 55 illustrates an overview of the Block A and Block B sections of the data center. Both blocks have reciprocating engines for emergency backup power. The only difference between the two blocks is that the Block B UPS supports enhanced LVRT whereas Block A does not, and the Block A load will transition to backup generation for voltage sags that Block B load can ride through. This is a practical situation as many UPS vendors are still in the process of rolling out enhanced LVRT features to their products. If Block A was constructed before Block B, the Block A UPS may be using an older model and/or firmware version which does not support the features.

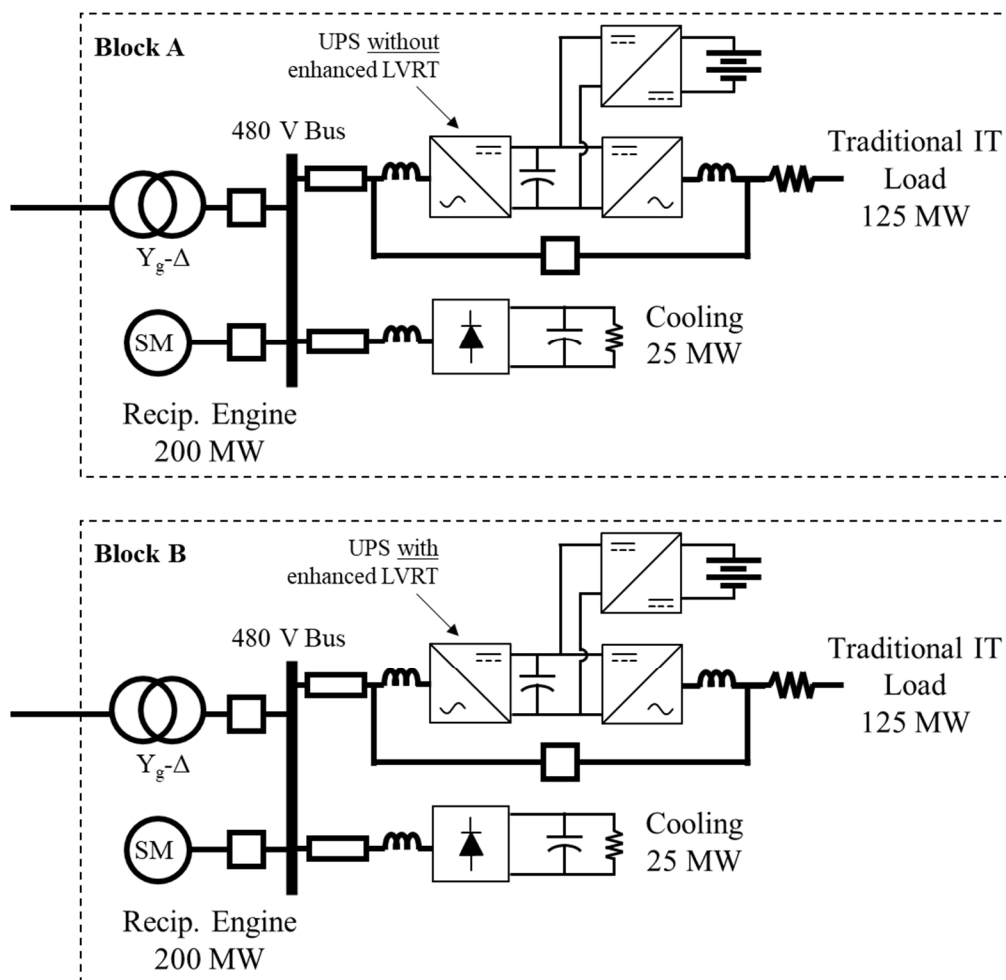


Figure 55: Single-line diagrams for Blocks A and B.

Figure 56 illustrates single line diagrams for Blocks C and D. The Block D load is co-located with a 150 MW GFM BESS which provides smoothing of the active power fluctuations from the AI training load. The GFM BESS is connected to the incoming MV feeder via a step-up transformer (rather than directly to the 480 V bus). This is because it is assumed that it is preferable to locate such a large quantity of batteries (much larger than the quantity within the racks themselves) outdoors to manage fire safety risks and maximize the indoor space that can be utilized by computing resources.

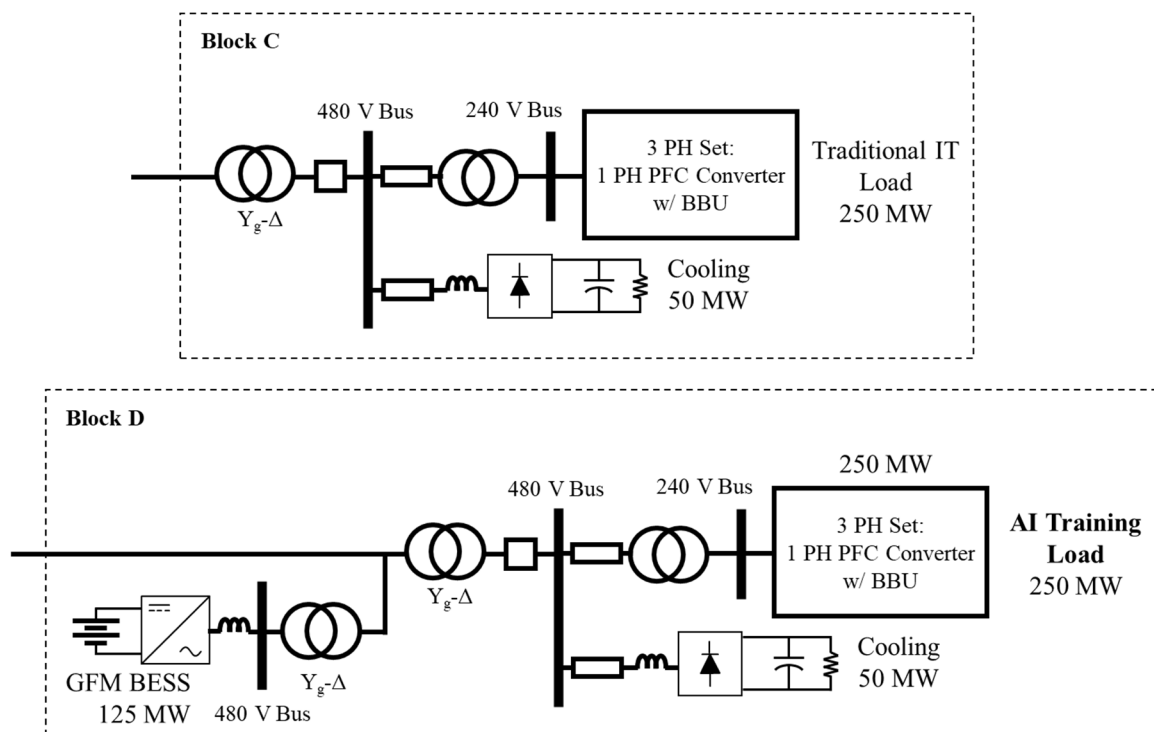


Figure 56: Single-line diagrams for Blocks C and D.

By default, the DML_DC4_Mixed system is set up to simulate a L-L grid fault lasting 100 ms. Each block of data center load responds differently to the fault, resulting in a POI-level behavior that is much more nuanced and complicated than that seen in the simpler data center models. This illustrates some of the complexity associated with evaluating LVRT performance of large data centers, and the importance of considering LVRT requirements early on in the data center design process in order to manage this complexity.

Figure 57 illustrates the voltage, current at the PCC during and immediately after the fault. Observe that the A- and B-phase voltages at the PCC fall to roughly 0.52 pu. Based on this, it is expected that a significant portion of the ITE will enter momentary cessation¹. Following the fault, the current magnitude is moderately reduced and slightly unbalanced, indicating that a portion of the load has disconnected, and disconnection has not been even among all three phases.

¹At the time of writing, thresholds for momentary cessation are generally in the range of 0.5 to 0.7 pu for data center power electronics. The logic usually operates based on RMS L-N phase voltage. Lower thresholds (e.g., 0.1 to 0.3 pu) may be achieved in the near future with further improvements to device control and/or energy storage.

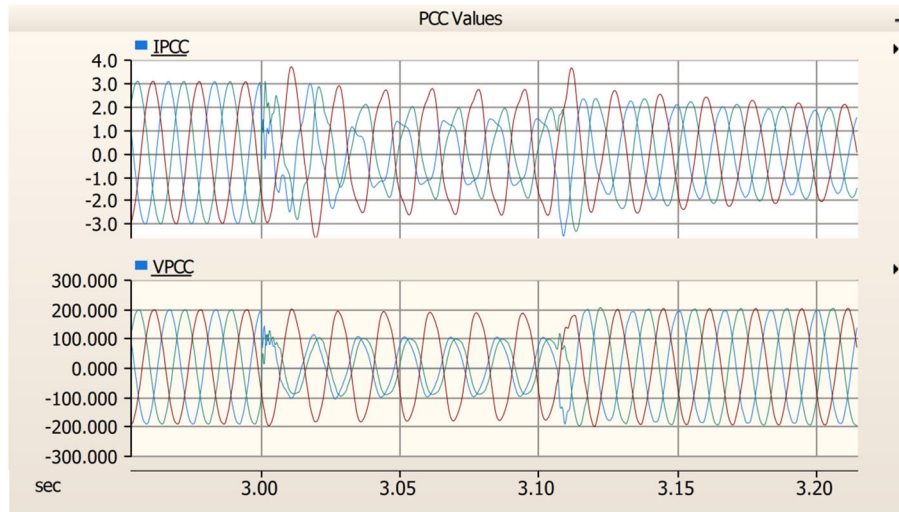


Figure 57: Instantaneous currents and voltages at the PCC during 100 ms L-L fault.

Figure 58 illustrates the effect of the L-L fault on the power consumption at the PCC (the top and middle plots) as well as on system frequency (the bottom plot). Roughly half of the facility load has ceased consumption following the fault, and roughly half of the load that ceases consumption resumes so by $t = 6$ s. For context—this response does not appear to meet ERCOT’s draft requirements for ride-through [99]. For undervoltages in the range of 0.5 to 0.8 pu, the minimum ride-through duration is 0.5 s. A reduction in active power consumption is permitted, but the facility must return to 90% of its pre-fault active power consumption (879 MW in this example) within 2 s of the voltage returning to nominal. Two seconds after voltage recovers, the active power consumption has returned to only 70% of the pre-fault consumption, and does not increase to a value above 90% by the end of the simulation.

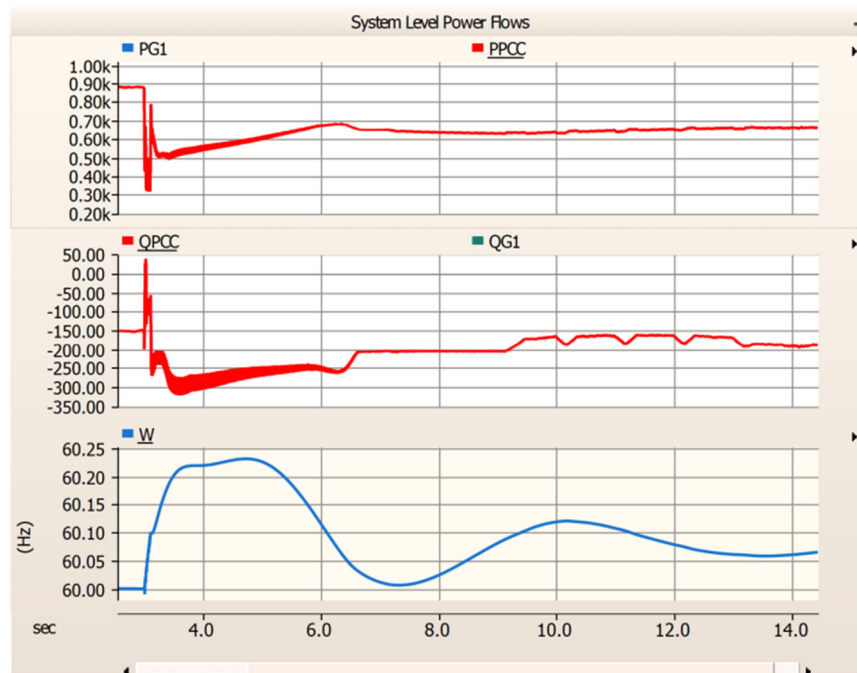


Figure 58: Impacts to PCC power flows and system frequency from 100 ms L-L fault.

The reactive power production of the facility increases significantly following the fault. This is because most of the reactive power production comes from an HV capacitor bank and harmonic

filters—the former is intended to offset the effects of voltage drop within the facility and the later to filter out drive harmonics. These ride-through the fault (no protection models have been added to them in this example), whereas the load, which caused the site’s transformers and cables to consume substantial reactive power, has been significantly reduced. The oscillation in reactive power present at $t = 9$ to 13 s is the result of the AI training, which has simply reached a particularly choppy stage in the training process at this point in the simulation. The BESS control used provides smoothing of active power only, and the active power fluctuations from the training are sufficient to cause variations in the voltage magnitude within the plant, even if they are mitigated downstream of the PCC.

To gain a more thorough understanding of how each block of data centers contributed to ride-through performance, the block-level power consumptions must be evaluated (Figure 59).

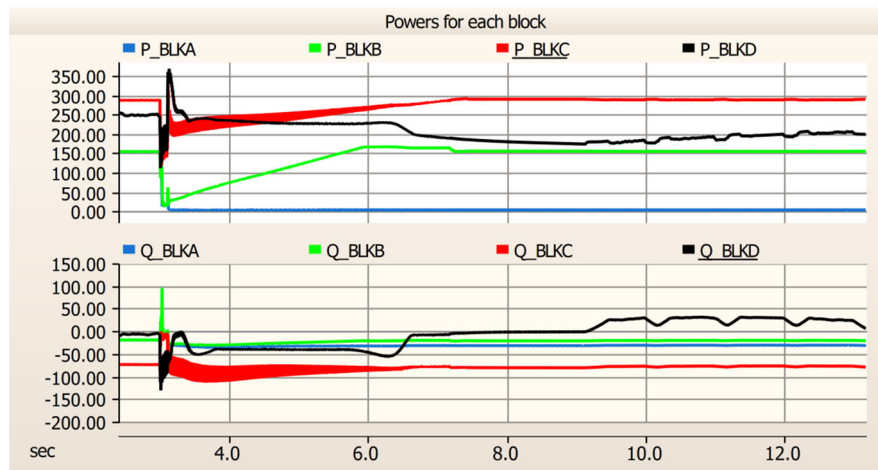


Figure 59: Impact to block-level power flows from 100 ms L-L fault.

Block A’s behavior is primarily determined by its use of legacy UPS with reduced LVRT capability. All the load in this block trips offline, presumably transferring to backup generation.

Block B enters momentary cessation but resumes relatively quickly—this is primarily the result of the UPS with enhanced LVRT.

Block C exhibits a moderate dip in active power consumption, followed by an oscillation in 3 PH active and reactive power lasting roughly 4 s. This oscillation is the result of unbalance—the set of power supplies connected on one phase pair enters momentary cessation whereas the others do not. However, the affected supplies resume their pre-fault active power consumption within 4 s.

Block D, due to the presence of a BESS, provides active and reactive power supporting during the fault. After the fault, Block D maintains active power consumption—the ITE trips offline but the BESS responds by absorbing active power (this is the natural behavior of the smoothing control employed). After several seconds, the ITE processing resumes and the slight ripple in active and reactive power resumes.

The automatic resumption of the AI training load is shown purely to demonstrate the model functionality (the associated time delay and ramp rate may be set arbitrarily)—this represents a scenario where the AI training process automatically resumes or restarts shortly after the fault.

While data center operators could choose to operate this way, this is likely not the case for many sites.

Additionally, this model does not represent the possibility that, even if all of the ITE in this block rides through, the training job itself may cease entirely due to tripping of other ITE that is participating in the training job and also affected by the fault¹. Thus, the ITE could suddenly cease active power consumption due to the job stopping, even if the power supply rides through. To mitigate this issue, some AI training hardware features a “load catch” feature, which will cause the hardware to continue consuming power (but not doing any useful computation) even if the compute job is suddenly stopped. However, it is possible that the site is using AI training hardware that does not possess this feature, or that the site operator is not using it (e.g., due to being unaware of its existence or importance for grid reliability).

NOTE: This model contains many sophisticated components and it takes approximately 1 hour to compute a 15 s simulation on a typical engineering workstation. Users are encouraged to use the “disable” option on individual data center blocks not being studied when conducting exploratory simulations or tuning parameters.

¹Effective synchronous training of AI models requires relatively low communications latency, and so all of the facilities involved in a particular training job are likely to be electrically close enough to be affected by the same voltage sag.

7.0 Component Models

DML contains PSCAD component definitions (in DML_Components.pslx) which represent individual devices or functions. This section describes all the component definitions in the library. The component definitions in the PSCAD library file are all schematic based (instead of code based) and nothing is encrypted or black-boxed. It is intended that the schematics themselves serve as documentation of the exact implementation, and this section is intended more to describe the models at a high level and call out application notes which are not obvious from the schematics alone.

Throughout the user guide, the font `Courier New` denotes the usage of a component definition name.

7.1 DC-DC Buck-Boost Converter (AVM) – `DC_bi_avm`

The `DC_bi_avm` component implements a DC-to-DC buck-boost converter, which can produce an output DC voltage ranging from roughly 0 to 2 times the input DC voltage. An AVM is used, a timestep of 50 μ s or less is recommended. It is a bidirectional converter. Such converters are sometimes used to interface batteries with inverters, as they can be used to provide controlled charging and discharging of the battery. In the DML, it is used to represent the UPS battery charger and interface either batteries or supercapacitors with DC distribution buses.

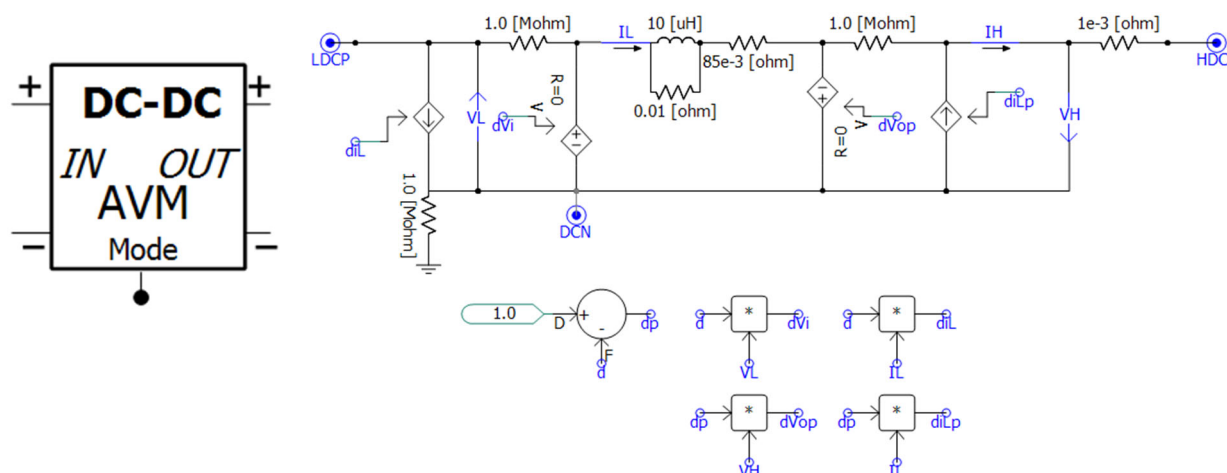


Figure 60: Icon (Left) and Main Electrical Schematic (Right) of `DC_bi_avm`.

The controller is built into the model and supports two control modes—either active power regulation or DC link voltage regulation. The `DC_bi_avm` component may be configured to operate in either one of these modes or to switch dynamically between the two, based on the control signal supplied to the “mode” input port. In either control mode, there is an additional parallel proportional controller operating based on DC link voltage. The primary purpose of this control path is to permit some level of DC link voltage support while operating in active power regulation mode, which is necessary to maintain tight DC voltage regulation when transitioning between control modes, especially during external disturbances like load steps or faults.

Table 15 describes the input parameters. To avoid needing to resize passive components, it is recommended to implement alternate power and voltage ratings using PSCAD’s built in scaling components.

Table 15: Input Parameters for DC_bi_avm Component.

Name	Units	Use
Converter On/Off	Boolean	Enable or disable firing of the IGBTs
Rated Power	MW	Define active power base for controls. By default, passives are sized for 1 MW.
Power set-point	pu	Target for power regulator, e.g., to represent battery charger setpoint. Positive values cause power flow from input to output; use a negative value to represent a battery charging load.
Controller objective	N/A	Three modes are supported: <u>DC Voltage</u> : A PI control is used to regulate duty cycle based on DC voltage error. <u>Active Power</u> : A PI control is used to regulate duty cycle based on DC voltage error. <u>Dynamic</u> : the converter operates in one of the two above modes, based on the value of input signal “mode,” switching between the two modes as commanded. Mode = 0 gives DC voltage regulation and mode = 1 gives active power regulation.
Nominal Output Voltage	kV	Define voltage base for controls. By default, passives are sized for 800 VDC input and 1200 VDC output.
Voltage setpoint	pu	Voltage reference for DC voltage regulation. In a UPS application, it is recommended to set this value to a slightly lower reference than that used by the rectifier. Otherwise, the battery control may completely take over active power supply during faults, reducing the rectifier’s active current to zero.
Max. Mod. Index	pu	Maximum duty cycle; can leave as 1 in most cases.
Power Regulator, Prop. Gain	pu	PI control gains used when operating in the active power control mode.
Power Regulator, Time Const.	s	
Voltage Measurement Time Const.	s	First order low-pass filter for output voltage regulator.
Voltage Reg. Prop Gain	pu	PI control gains used when operating in the DC voltage regulation control mode.
Voltage Reg., Time Const.	s	
Voltage Reg. Feedfwd Gain	pu	Gain of additional proportional controller for DC voltage regulation, active regardless of control mode (active power or DC voltage regulation).

7.2 DC-DC Buck-Boost Converter (SWM) – DC_bi_swm

The `DC_bi_swm` component is a SWM alternative to `DC_bi_avm`. It has the same set of input parameters (see Table 15).

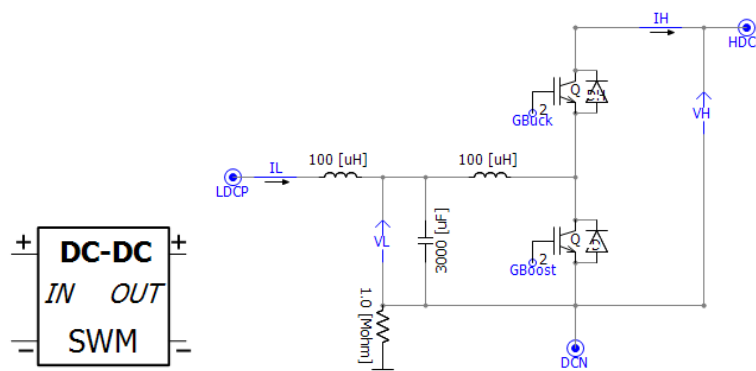


Figure 61: Icon (Left) and Main Hardware Schematic (Right) for `DC_bi_swm` Component.

7.3 Reciprocating Engine Genset – gen_recip

The `gen_recip` component represents a synchronous generator powered by a reciprocating internal combustion engine, which may be burning diesel, gas, or natural gas. The model supports both grid-connected¹ and islanded operation.

The governor uses one of two different control strategies, based on a control signal input meant to indicate whether the generator is operating in islanded or grid-connected mode. In islanded mode, speed is regulated to the set reference (e.g., 60 Hz) using a PI control. In grid-connected mode, active power is regulated to the set reference and speed is regulated using a proportional droop control.

The `gen_recip` component includes a basic underspeed protection, which is chiefly relevant when starting loads during islanded operation. The diesel engine will stall if its speed is significantly reduced during such circumstances. Users may observe the stalling behavior by setting the underspeed protection to have either a very low pickup value or a long time delay.

¹Many commercially available reciprocating engine gensets are not suitable for grid-connected operation in practice.

Table 16: General Parameters for `gen_recip` Component.

Name	Units	Use
Generator MVA Rating	MVA	Apparent power rating for generator.
Generator Voltage Rating	kV LN RMS	Generator nominal voltage. This is L-N voltage, not L-L voltage.
Engine MW Rating	MW	Active power rating for engine. Should be less than or equal to the generator MVA rating. The governor control operates on this power base, not the generator MVA rating.

Table 17: Governor Parameters for `gen_recip` Component.

Name	Units	Use
Control mode	Boolean	Determines governor control mode (0 = grid connected, 1 = islanded)
Engine time const.	s	Time constant representing response of fuel system and engine torque to changes in fuel flow command.
Governor Prop. Gain	pu	Proportional gain for speed regulator (active in islanded mode).
Governor Int. Time Const.	s	Integral time constant for speed regulator (active in islanded mode).
P reg. prop. gain	pu	Proportional gain for active power regulator (active in grid-connected mode).
P reg. int. time const.	s	Integral time constant for active power regulator (active in grid-connected mode).
Speed droop	pu	Droop gain for frequency regulation (active in grid-connected mode).

Table 18: Exciter Parameters for `gen_recip` Component.

Name	Units	Use
Regulator gain	pu	Proportional gain of the automatic voltage regulator.
Maximum regulator output	pu	Maximum field voltage output for the exciter
Minimum regulator output	pu	Minimum field voltage output for the exciter
Load compensating resistance	pu	Resistance used for load-drop compensation of the voltage regulator
Load compensating reactance	pu	Reactance used for load-drop compensation of the voltage regulator
Exciter time const.	s	Time constant representing the response of the excitation circuit
Volts Per Hz Droop	pu	Change in voltage reference per unit speed deviation (e.g., a value of 2 will cause the voltage reference to be reduced by 2% for every 1% reduction in speed). This feature helps the generator accept large load blocks without engine stalling.

Table 19: Initialization Parameters for `gen_recip` Component.

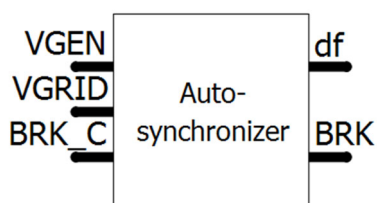
Name	Units	Use
Initial active power output	pu	Sets initial outputs for governor controls to reduce startup transients. If unsure, set to a moderately high value (e.g., 0.7 pu) to avoid engine stalling.
Machine enable signal name	Boolean	PSCAD standard signal for machine startup, generator modeled as a Thevenin source and exciter control frozen until this signal = 1.
Swing equation enable signal name	Boolean	PSCAD standard signal for machine startup, generator speed is frozen at 1 pu until this signal = 1.

Table 20: Protection Parameters for `gen_recip` Component.

Name	Units	Use
Underspeed trip threshold	pu	Speed below which underspeed protection begins timing.
Underspeed trip time delay	pu	If generator speed drops below the trip threshold for this time duration, the generator will be tripped offline.

7.4 Generator Autosynchronizer – `gen_sync`

The `gen_sync` component represents an autosynchronizer, which is used to bring an islanded generator's voltage phase angle into alignment with the grid voltage phase angle prior to circuit breaker closure (Figure 62). It operates based on two sets of three-phase voltages (VGEN and VGRID) assumed to be taken on two sides of a circuit breaker. Received commands for breaker position (BRK_C) are supervised by synchronization check logic and passed to the output, BRK.

Figure 62: Icon for the `gen_sync` component.

Received commands to open the breaker are passed without modification, but commands to close the breaker are passed only if the voltages meet user-specified tolerances for phase, frequency, and magnitude difference. When a close command is received, a speed regulation control loop is activated and produces per-unit speed deviation command, “df.” This control operates based on the phase angle difference and assumes that the speed deviation command is being sent to the governor of the generator(s) on the side of the breaker where VGEN is measured.

Figure 63 illustrates a successful autosynchronization. At $t = 30$ s, an islanded diesel engine generator (`gen_diesel`) is subjected to a large step load which results in a temporary underfrequency condition. The engine successfully restores the frequency to nominal conditions but, as expected, the voltage phase angle differs substantially from the grid voltage angle. At $t = 60$ s, the breaker providing grid connectivity is commanded to close. This activates the speed control of the autosynchronizer, which slightly accelerates the machine over the course of roughly 60 s. Once the phase angle difference is small enough (below 10° for 5 seconds, in this example) the breaker closure is executed. For more details on use of this component with generator models, refer to example model `DML_Gen_Demo`.

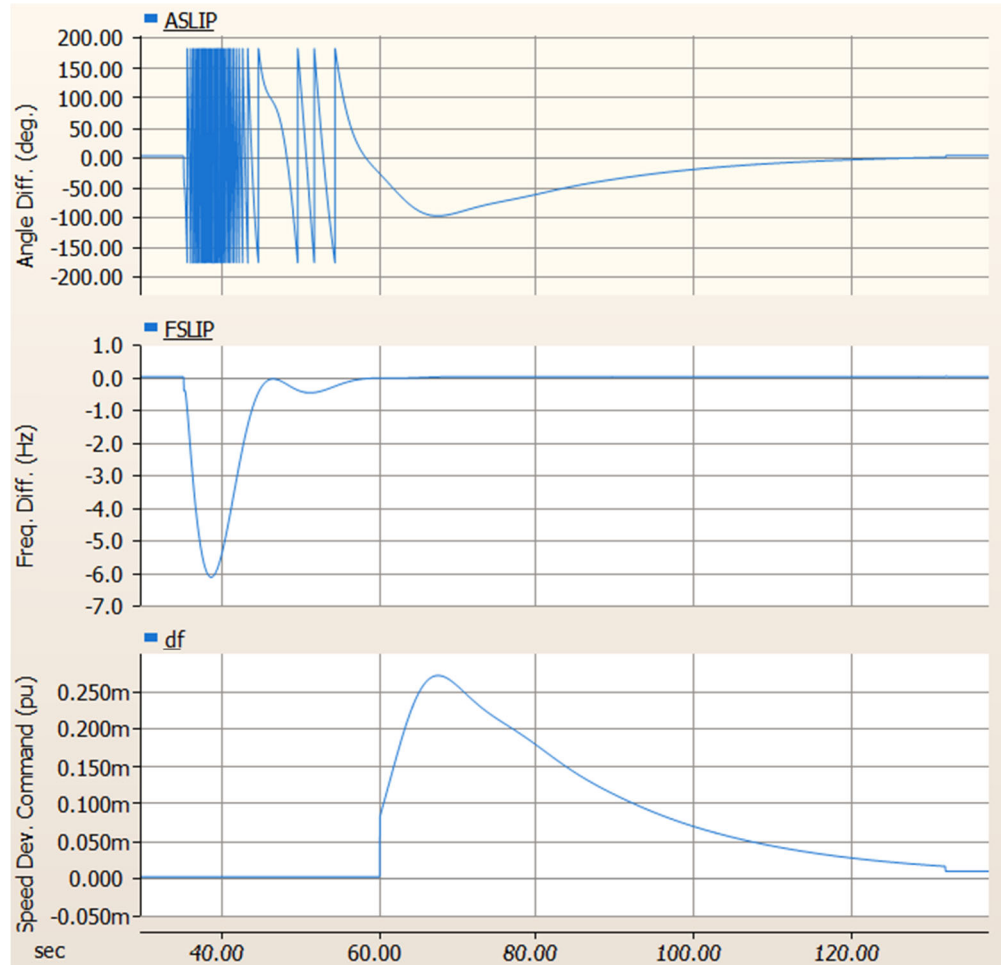


Figure 63: Autosynchronizer quantities during islanded operation ($t = 30$ to 60 s) and synchronization process ($t = 60$ to 135 s).

The response of generator voltage phase angle to changes in speed reference tends to be lightly damped, and it is necessary to use very low gains for the synchronizer control to avoid unstable operation. As a result, synchronization time can be long in terms of EMT simulation (e.g., 60 s). If the synchronization process is not a key aspect of the analysis, users may consider using unrealistically relaxed limits for frequency and phase synchronization purely for the purpose of simulation expediency.

A three-phase PLL is used to obtain the frequency and phase measurements, and it may be necessary to relax the frequency and/or phase tolerances to achieve synchronization if one of the two voltage sources has appreciable unbalance.

Table 21: General Parameters for `gen_sync` Component.

Name	Units	Use
Nominal frequency	Hz	Rated electrical frequency of the supplied voltage measurements
Nominal voltage	kV L-L RMS	Rated voltage magnitude of the supplied voltage measurements
Freq. meas. time const.	s	Time constant of the low-pass filter applied to frequency measurements
Startup time	s	The autosynchronizer is bypassed and all input breaker closure commands are passed to the output until simulation time exceeds this value.

Table 22: Speed Regulator Parameters for `gen_sync` Component.

Name	Units	Use
Speed reg. prop. gain	pu	Proportional gain for speed regulation, must be small (e.g., 1e-3) to obtain stable operation.
Speed reg. int. time const.	s	Time constant of integrator for speed regulation, must be very large (e.g., 1e6) to obtain stable operation.
Speed reg. max dev.	pu	Limits for speed regulator, may be kept at small values as the peak speed deviation necessary to eliminate phase error is very small.

Table 23: Synch Check Parameters for `gen_sync` Component.

Name	Units	Use
Max. angle dev.	deg.	Maximum acceptance voltage phase angle difference to permit breaker closure.
Angle check pickup time	s	Phase angle difference requirement must be satisfied for this time difference to permit breaker closure.
Max. freq. dev.	pu	Maximum acceptance voltage frequency difference to permit breaker closure.
Freq. check pickup time	s	Frequency difference requirement must be satisfied for this time difference to permit breaker closure.
Max. volt dev.	pu	Maximum acceptance voltage magnitude difference to permit breaker closure.
Volt. check pickup time	s	Voltage magnitude difference requirement must be satisfied for this time difference to permit breaker closure.

7.5 GFM Droop Control – gfm_droop

The `gfm_droop` component contains control loops necessary to implement GFM droop control in a three-phase inverter. It also includes optional controls for AC voltage regulation and PLL-based angle locking (which improves large-signal stability). It is used as a component in the GFM inverter models which use the droop-based approach for obtaining GFM operation. See `inv_gfm_droop_avm` for a complete inverter model which uses this component. All input and output signals in per-unit.

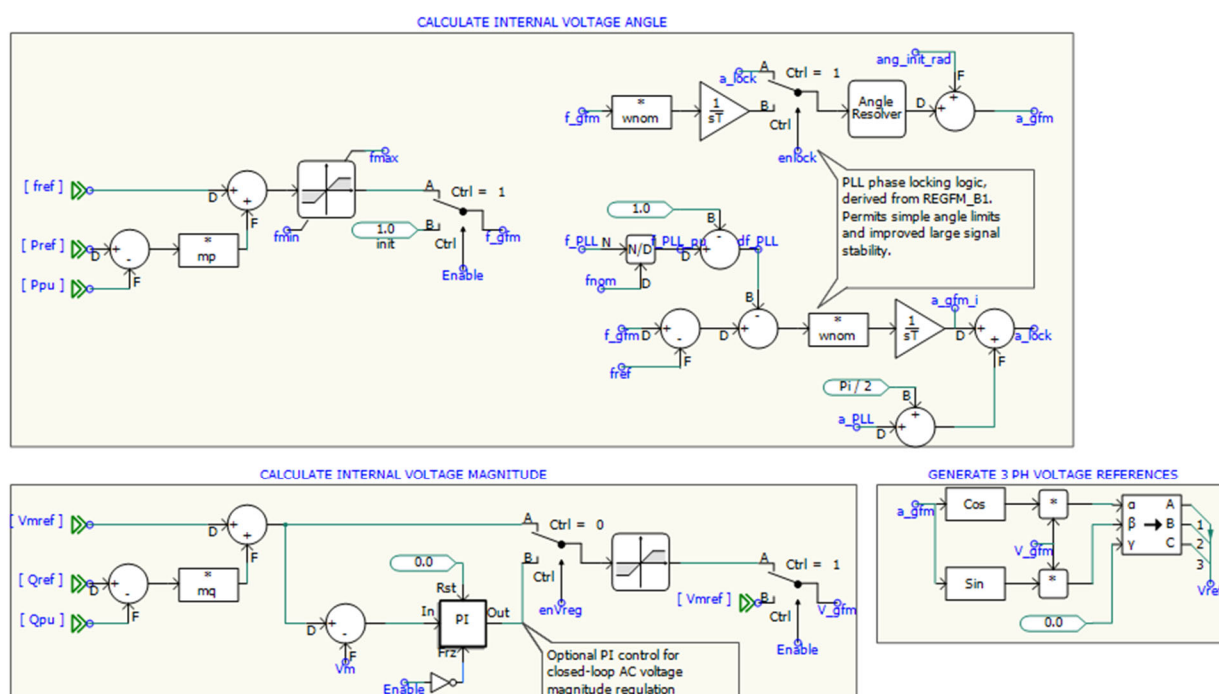


Figure 64: Main Control Elements for the `gfm_droop` Component.

Table 24: Input Parameters for `gfm_droop` Component.

Name	Units	Use
Nominal frequency	Hz	Defines AC frequency base
Droop Gain, Real Power	pu	N/A
Droop Gain, Reactive Power	pu	N/A
Maximum frequency	pu	N/A
Minimum frequency	pu	N/A
Enable PLL lock and angle limits?	Boolean	Enables a PLL input to the voltage angle control loop which allows for locking of the GFM voltage angle during faults. This improves the large-signal stability of the control and reduces the need for the Stage 2 current limit. Based on the approach used in REGFM_B1 [100], adapted for droop [101].
Max. power angle	deg.	Maximum positive sequence voltage angle of inverter terminal voltage relative to filter output voltage. Only enforced if PLL lock is enabled.
Min. power angle	deg.	Minimum positive sequence voltage angle of inverter terminal voltage relative to filter output voltage. Only enforced if PLL lock is enabled.
Enable AC Volt. Reg.?	Boolean	Enables closed-loop regulation of AC voltage. Not recommended to enable if the Stage 2 I limit is enabled.
Max. AC Voltage Command	pu	Upper limit for positive sequence voltage magnitude commanded by droop control.
AC Volt. Reg. Prop. Gain	pu	Proportional gain for optional AC voltage regulator.
AC Volt. Int. Time. Const.	s	Integral time constant for optional AC voltage regulator.
Startup time	s	Until simulation time exceeds this value, output voltage magnitude, frequency, and angle are forced to the voltage magnitude reference, nominal frequency, and initial voltage angle, respectively.

7.6 GFM Droop Control w/ Vdc Reg. – `gfm_droop_vdc`

For most cases where a GFM inverter is applied, it is assumed that DC link voltage is regulated to a constant value by some other component (e.g., the DC/DC converter for a battery). The `gfm_droop_vdc` component is a variant of `gfm_droop` that handles the less common (but sometimes necessary) condition where the GFM inverter must contribute to DC link voltage regulation.

The `gfm_droop_vdc` component uses a DC voltage rather than AC active power to regulate its AC frequency. A proportional-derivative control (rather than a proportional control) is used to provide additional phase lead and improve the control's transient response [102].

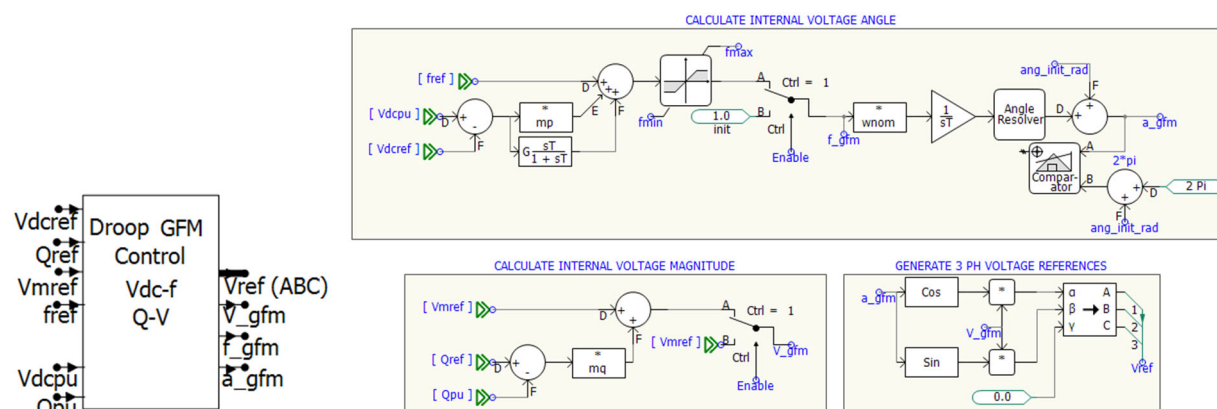


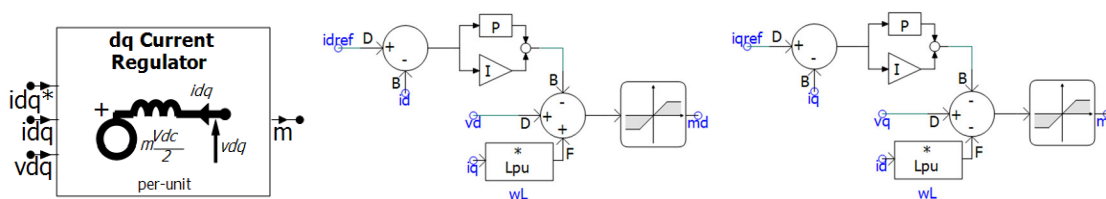
Figure 65: Icon (Left) and Main Control Diagram (Right) for `gfm_droop_vdc` Component.

Table 25: Input Parameters for `gfm_droop_vdc` Component.

Name	Units	Use
Nominal frequency	Hz	Defines AC frequency base
Droop Gain, DC Voltage	pu	N/A
Deriv. Gain, DC Voltage	pu	N/A
Deriv. Time Const.	s	N/A
Maximum frequency	pu	N/A
Minimum frequency	pu	N/A
Initial voltage angle	degrees	Adjust this to obtain desired power flow at startup. If this angle differs too much from the bus voltage angle where the associated inverter is connected, the inverter may not successfully synchronize.
Startup time	s	Until simulation time exceeds this value, output voltage magnitude, frequency, and angle are forced to the voltage magnitude reference, nominal frequency, and initial voltage angle, respectively.

7.7 dq-Domain current regulator – `ireg`

The `ireg` component implements a dq-domain current regulator, which varies a three-phase inverter's dq-domain modulation index to achieve a given current reference. This is a common control loop in IBR models as it allows for fast current limiting during grid faults. All input and output signals are in per unit. The `ireg` component will limit the modulation indices produced to within ± 2 pu but has no built-in current limiting.

Figure 66: Icon (Left) and Main Controls (Center, Right) for the *ireg* Component.Table 26: Input Parameters for *ireg* Component.

Name	Units	Use
Kp, Current Regulator	pu	Proportional gain for PI controllers
Ti, Current Regulator	s	Integral time constant for PI controls
AC Side Inductance	pu	Total series inductance between node where v_{dq} is measured and the AC terminals of the inverter (which is producing an AC voltage as defined by m_d and m_q).

Table 27: Input Parameters for *ilim_3p* Component.

Name	Units	Use
Current limit	pu	N/A
Nominal frequency	Hz	Defines time window for RMS calculation.

7.8 dq-Domain Current Limiter – *ilim_dq*

The *ilim_dq* component is used to limit a set of d- and q-axis current references such that the magnitude of the dq-domain current space vector is limited. This is done by choosing to either prioritize maximizing the d-axis current or the q-axis current. This component is used to limit the current references produced by an outer loop control prior to sending them to a current regulator (e.g., *ireg*).

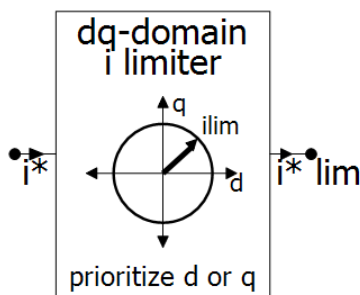
Figure 67: Icon for the *ilim_dq* Component.

Table 15 describes the input parameters for the *ilim_dq* component.

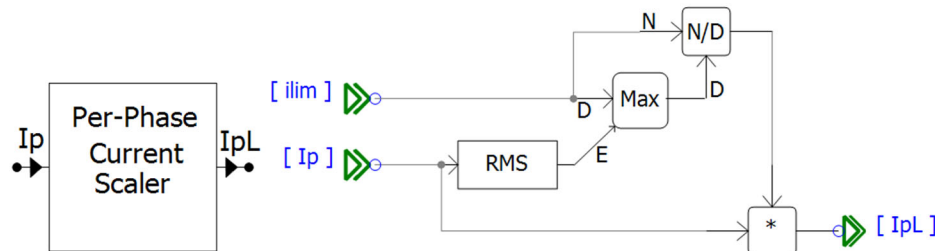
Table 28: Input Parameters for *ilim_dq* Component.

Name	Units	Use
Current magnitude limit	pu	N/A
Prioritize d-axis current?	Boolean	A value of 1 results in d-axis prioritization. This field is a variable, so variable prioritization (e.g., q-axis priority only during voltage sags) is supported.

7.9 Per-Phase Current Scaler – *ilim_pp*

The *ilim_pp* component is used to limit a single current reference. It is used to provide current limiting for single phase AC/DC converters.

Figure 68 illustrates the icon and schematic for the *ilim_pp* component and Table 29 describes the component's input parameters.

Figure 68: Icon (Left) and Schematic (Right) for *ilim_pp* Component.Table 29: Input Parameters for *ilim_pp* Component.

Name	Units	Use
Current limit	pu	N/A
Nominal frequency	Hz	Defines time window for RMS calculation.

7.10 3 PH Inverter, AVM – *inv_avm*

The *inv_avm* component implements an AVM representation of a two-level voltage-source converter. This AVM is more sophisticated than many AVMs in that it includes built-in representation of PWM-level current clipping [103]. This is the purpose of the shunt current sources, which are active only when the current clipping is. If this feature is disabled, the model is equivalent to the commonly used AVM.

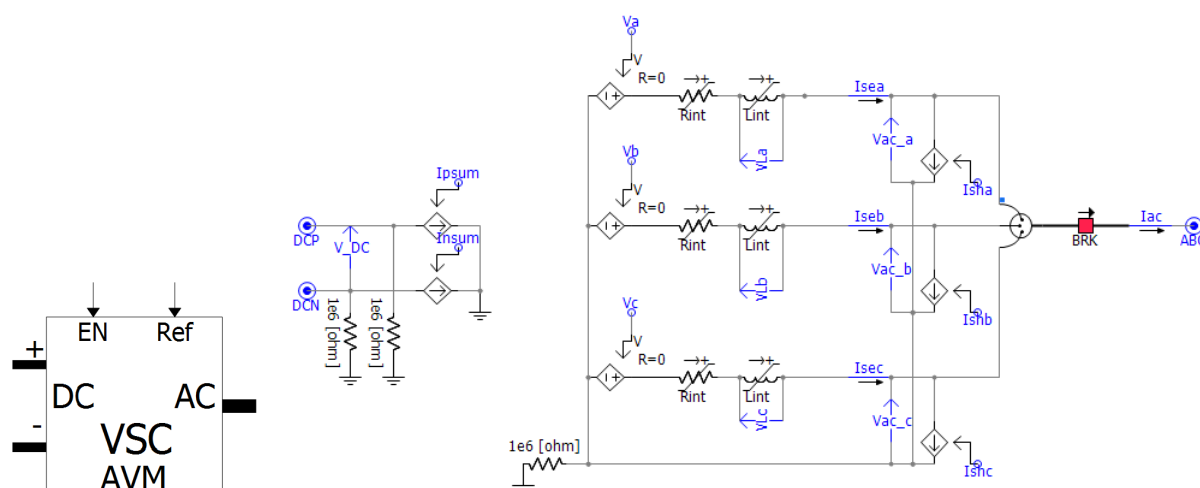


Figure 69: Icon (Left) and Main Hardware Schematic (Right) for `inv_avm` Component.

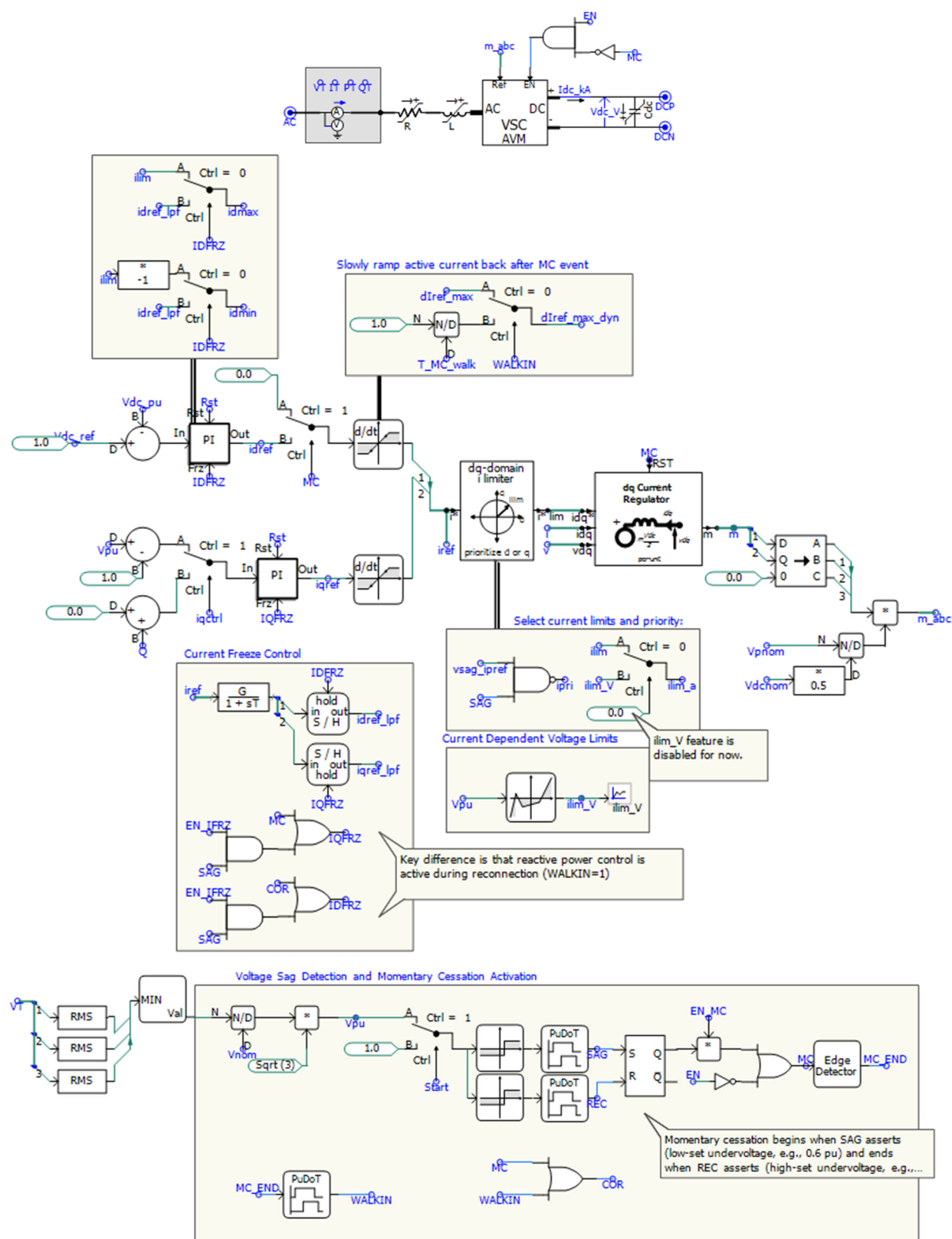
The inverter models that use the `inv_avm` component (e.g., `inv_gfl_avm` or `inv_gfm_droop_avm`) have built-in controls to derive input parameters for `inv_avm` without additional user input. These controls assume the inverter is operating at low-voltage (<1 kV). If using this model to represent high-voltage inverters (e.g., a 500 kV HVDC converter), the user will need to increase the internal resistance and inductance and tune them to match the appropriate SWM. However, this is unnecessary for the data center use cases that are the DML's focus.

Table 30: Input Parameters for `inv_avm` Component.

Name	Units	Use
Internal Resistance	Ω	Value of R_{int} , a value equal to 10,000 times the simulation timestep in seconds works well for low-voltage inverters.
Internal Inductance	H	Value of L_{int} , a value equal to the simulation timestep in seconds works well for low-voltage inverters.
Enable Inverter-Level Current Limit?	Boolean	Enables current clipping. If zero, the shunt current sources are forced equal to 0 amperes and the component is equivalent to the traditional AVM.
Current Limit	kA	Instantaneous current will be clipped to this value. It should be at least ~20% greater than any software-level current limiting.

7.11 3 PH Inverter, GFL – `inv_gfl_avm`

The `inv_gfl_avm` component represents a three-phase inverter with a grid following control. It is intended to represent small inverter-based generation or inverter-based loads, where more advanced grid support functions are seldom implemented. No plant-level controller is included.


 Figure 70: Main Hardware Schematic and Major Control Elements for `inv_gfl_avm`.

An AVM is used and a timestep of 50 μ s or less is recommended. The component used for the AVM is `VSC_AVM` component.

A three-phase PLL is used to track the AC side voltage and control is performed in the dq domain. The d-axis current reference is determined by a DC voltage regulator. The q-axis current reference may be controlled using either a reactive power regulator or an AC voltage magnitude regulator. Based on these current references, the voltage references are determined using a dq -domain current regulator (the `ireg` component), which also provides current limiting. Unless there is an AC side voltage sag, the d-axis current is prioritized (using the `ilim_dq` component).

The component supports several different AC-side low-voltage ride-through modes, based on a user-defined threshold for voltage sags. The component can be configured to prioritize q -axis current during voltage sags, providing reactive power support (if AC voltage regulation is also enabled). Momentary cessation with a controlled ramp-rate as well as constant current operation are also supported.

Table 31 and Table 32 describe the different input parameters for the `inv_gfl_avm` component. To avoid needing to resize passive components, it is recommended to implement alternate power and voltage ratings using PSCAD's built in scaling components.

Table 31: Ratings-Related Input Parameters for `inv_gfl_avm` Component.

Name	Units	Use
Nominal Apparent Power	MVA	Defines apparent power base for controls
Nominal L-L RMS Voltage	kV	Defines AC voltage magnitude base for controls
Nominal AC Frequency	Hz	Defines frequency base for controls
Nominal DC Link Voltage	kV	Defines DC voltage base for controls
AC Current Limit, pu	pu	Defines limit for current regulator limiter
DC Link Capacitance	μ F	Usually ranges from 1 to 10 mF per MVA
AC Side Inductance, pu	pu	Usually ranges from 0.05 to 0.2 pu.
Startup Time Delay, s	s	Until simulation time exceeds this value, controls are frozen and inverter AC voltage forced to magnitude of 1 pu and angle of 0 degrees.

Table 32: Controller-Related Input Parameters for `inv_gfl_avm` Component.

Name	Units	Use
Current Regulator, Proportional Gain	pu	PI control gains for inner control loop
Current Reg., Integral Time Constant	s	
Current Ref., Max Rate of Change, pu/s	pu/s	Limits the rate at which current reference can change, effects most prominent when IBR changes control mode when an AC voltage sag begins or ends.
DC Volt. Reg., Prop Gain, pu	pu	PI control gains for DC voltage outer control loop
DC Volt. Reg., Int Time Const., pu	s	
Reactive Power Control Method?	N/A	Drop-down menu—select control objective for q-axis current to be either reactive power or AC voltage magnitude regulation. Internally, Q_{ref} is set to 0 and $V_{ac,ref}$ is set to 1 pu.
React. Pow. Prop Gain	pu	PI control gains for reactive power outer control loop
Reac. Pow. Int. Time Const	s	
Voltage Sag Threshold	pu	Magnitude threshold below which LVRT-related functions activate. Operates based on minimum of the three RMS line-to-ground voltages.
Enable Momentary Cessation?	Boolean	If nonzero, voltage sags will cause the VSC to be blocked for the duration of the sag (AC current will drop to zero) and the current commands will ramped back in at a set rate after the sag ends.
Freeze Current Ref. During Voltage Sags?	Boolean	If nonzero, voltage sags will cause the current reference commands to be frozen for the duration of the sag, resulting in constant current operation.
Momentary Cess. Pickup Time Delay	s	Time duration for which voltage sag must persist to trigger start momentary cessation
Momentary Cess. Reconnection Voltage	pu	After momentary cessation is entered, it will remain active until voltage magnitude recovers beyond this threshold. This value must be greater than or equal to the Voltage Sag Threshold.
Momentary Cess. Dropout Time Delay	s	Time duration for which voltage magnitude must exceed the reconnection voltage to trigger end of momentary cessation.
Momentary Cess., Walk-In Time	s	Time duration over which the AC current is ramped back in after the end of momentary cessation.

7.12 3 PH Inverter, GFM, Droop Control, AVM – `inv_gfm_droop_avm`

The `gfm_ibr_droop_avm` component represents a three-phase inverter that uses a droop-based GFM control (`gfm_droop`). The inverter is represented with an AVM (`inv_avm`). A timestep of 50 μ s or less is recommended.

A single-layer control is used, meaning that there is no voltage or current regulator used. Fast current limiting is done at the PWM-level using hysteresis control. An optional, slower current limiter (`stage2_ilim`) may be used as well. This second stage can improve the inverter's ability to remain synchronized during close-in, long-lasting faults.

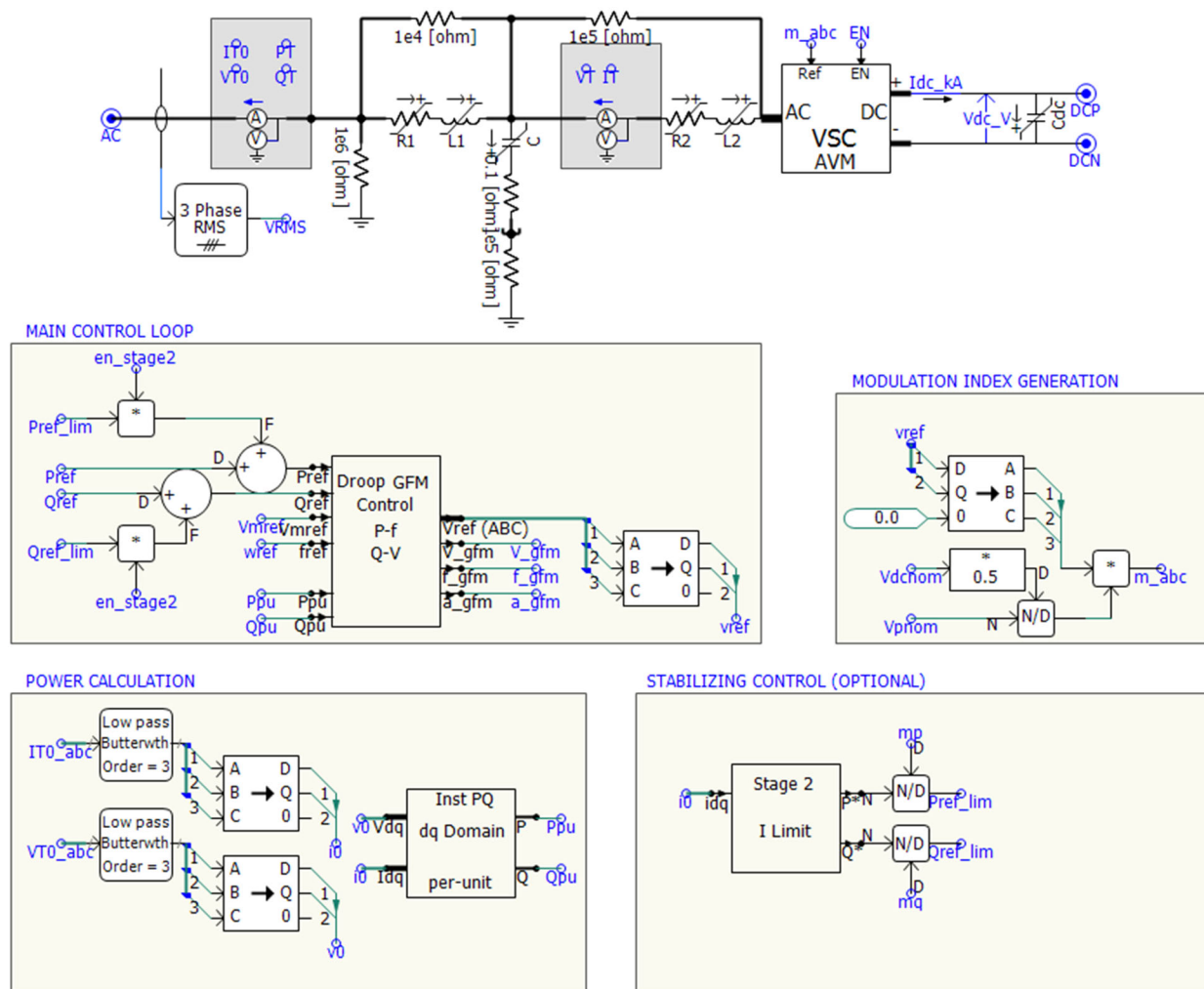


Figure 71: Hardware Schematic (Top) and Major Control Features (Bottom Four Rectangles) for `inv_gfm_droop_avm` Component.

NOTE: The AVM present in `inv_avm` differs from the traditional AVM in that it supports an AVM representation of hysteresis current limiting, such as that used in `gfm_ibr_droop_swm`.

Table 33: Ratings-Related Input Parameters for `inv_gfm_droop_avm` Component.

Name	Units	Use
Nominal Apparent Power	MVA	Defines apparent power base for controls
Nominal Voltage	L-L RMS kV	Defines AC voltage magnitude base for controls
Nominal AC Frequency	Hz	Defines frequency base for controls
Nominal DC Link Voltage	kV	Defines DC voltage base for controls
DC Link Capacitance	μ F	Usually ranges from 1 to 10 mF per MVA
LCL Filter Total Inductance	pu	Usually ranges from 0.05 to 0.2 pu.
LCL Filter Capacitance	μ F	N/A
Startup Time Delay, s	s	Until simulation time exceeds this value, controls are frozen and inverter AC voltage forced to magnitude of 1 pu and angle of 0 degrees.

Table 34: Control-Related Input Parameters for `inv_gfm_droop_avm` Component.

Name	Units	Use
Frequency droop	pu	Proportional gain for $P - f$ droop control
Voltage droop	pu	Proportional gain for $Q - V $ control
Power calculation, Time Const.	s	First-order low-pass filter for active and reactive power calculations. Strongly affects the bandwidth of droop control.
Enable Current Clipping?	Boolean	Make nonzero to enable “clipping” of instantaneous currents above user-set limit.
AC Current Limit	pu	Defines current limit for current clipping. A value of at least 1.2 pu is recommended to avoid stability issues.
Enable Stage 2 I Limit?	Boolean	Make nonzero to enable stabilizing control (<code>stage2_ilim</code>), which has built-in current limit of 1 pu.

7.13 3 PH Inverter, SWM – `inv_swm`

The `inv_swm` component implements a two-level IGBT-based voltage-source converter. The IGBTs themselves are approximately ideal and basic triangular PWM control is included.

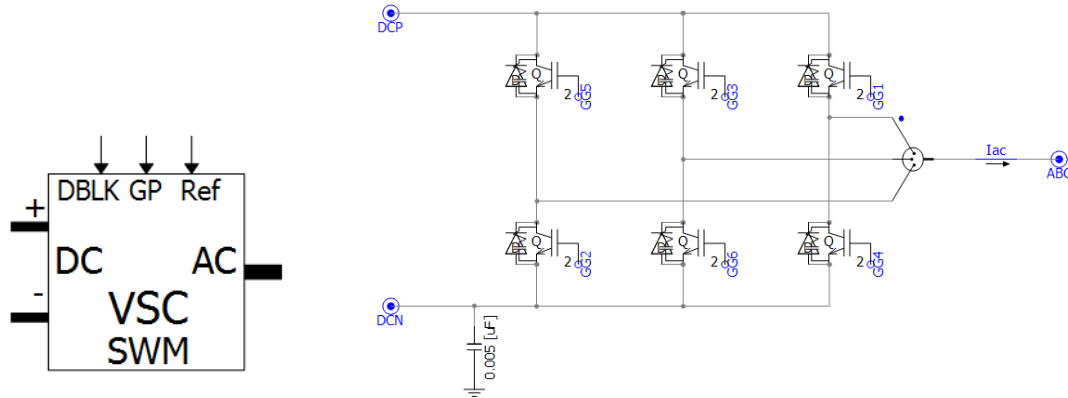


Figure 72: Icon (Left) and Main Hardware Schematic (Right) for `inv_swm`.

Both the DBLK and GP inputs permit blocking of the IGBT firing. DBLK is a 1-dimensional signal and is used to enable or disable all six switches. GP is a 6-dimensional signal used to block individual switches, which permits convenient representation of device-level current limiting such as the current clipping used in the `inv_gfm_droop_swm` component.

The only input parameter for `inv_swm` is the carrier frequency for the PWM, given in Hz.

7.14 Variable AI Training Load – `load_ai_train`

Training and inference for large AI models is most quickly done by operating large quantities (e.g., 200,000+) computing devices in parallel. The actual compute burden varies rapidly as individual computing tasks are completed and new tasks are initiated. Aggregated at a facility level, this corresponds to very large and rapid oscillations in power demand. The `load_ai_train` component is a convenient tool for producing very simplified versions of oscillating waveforms. Its simplicity makes it convenient for producing conservative waveforms targeting specific frequencies. If actual load profile data is available, use the `load_playback` component instead.

The `load_ai_train` component does not explicitly represent AI training processes. It is a time varying resistor, which cycles between large and small values based on the frequencies set by the user. If the component is connected to a bus with a relatively constant voltage magnitude (e.g., the output of a double-conversion UPS or a tightly regulated DC bus voltage), this simplified approach is appropriate. However, it is likely a poor representation of the training processes' response to large voltage deviations.

Table 35: Input Parameters for `load_ai_train` Component.

Name	Units	Use
Nominal AC Voltage, kV RMS L-L	kV	Defines voltage base
Nominal Power	MW	Defines active power base
Compute/Rest Frequency (Slow)	Hz	Frequency of slow variations in demand
Compute Block Frequency (Fast)	Hz	Frequency of fast variations in demand. Should be an integer multiple of the Compute/Rest Frequency (e.g., 10, 16, or 20).
Compute Loading	pu	Active power consumed at high loading level.
Resting Load	pu	Active power consumed at low loading level.
Load Step Time Constant	s	Time constant of first-order low-pass filter applied to time-varying resistance. A value of several milliseconds approximates the filtering effect of the low voltage power supplies.
Start Time	s	Load is fixed to compute loading level until simulation time exceeds this value.

Figure 73 illustrates the active power waveform the `load_ai_train` component is intended to implement, with annotations indicating how the input parameters relate to the waveform.

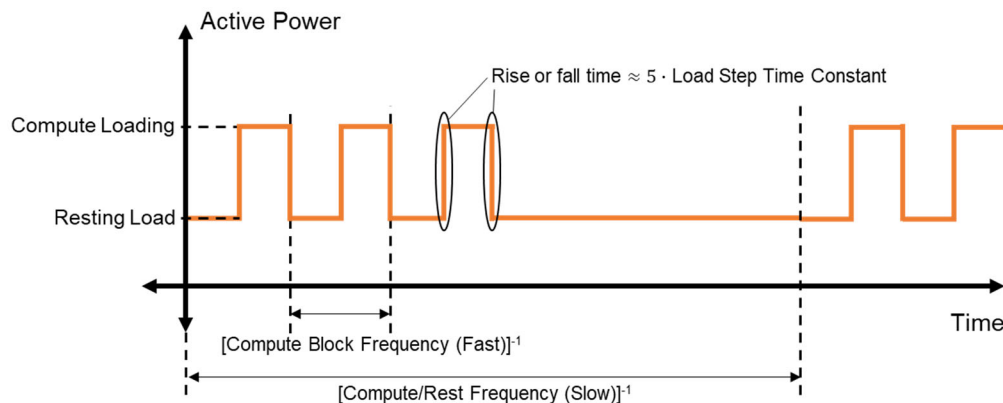


Figure 73: Simplified AI Training Waveform and Relationship with `load_ai_train` Component Parameters.

7.15 Playback-Based Electronic Load – `load_playback`

The `load_playback` component is intended to be used in conjunction with PSCAD's built in "File Read" component to play user-specified active power waveforms into a system model. This can be used to evaluate how rapidly-varying data center demand variations affect nearby devices such as generators and other power electronics.

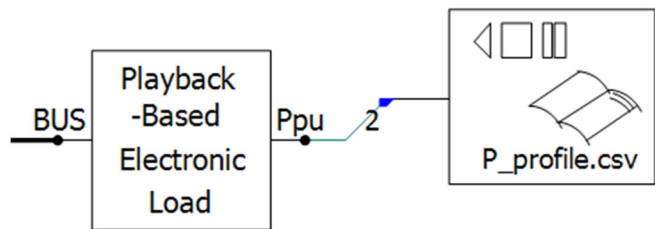


Figure 74: Icon for `load_playback` Component and Intended Connectivity with PSCAD's File Read Component.

The File Read component is not implemented within the `load_playback` component due to compile-time issues related to generation of links to external files within a submodule. It is recommended to format the desired load profile data into a two-column .csv file, with the first column containing sample times and the second column containing per-unit active power demand. It should then be placed in the same file folder as the PSCAD project in use. Figure 75 illustrates the recommended settings for the File Read component. The delay value (in seconds) should be set large enough to allow the model to initialize before beginning playback.

Name for Identification	
File Name	P_profile.csv
Path to the File Given as	relative path
Number of Columns in the Output File	2
Sampling Time Information	first columns contains sampling time
At the End of Datafile	rewind and replay again
sampling Frequency	6400.0 [Hz]
Delay	1
Before the Delay	zero

Figure 75: Recommended Parameters for File Read Component for Use with `load_playback`.

The `load_playback` component includes current limiting and momentary cessation functions, which allow for a basic representation of an electronic load's response to large changes in terminal voltage magnitude. These are simplified implementations of the more detailed fault responses present in the `gfl_ibr` component and allow the user to include external load profiles in scenarios including faults while avoiding the wildly unrealistic current waveforms or numerical stability issues that simple constant power loads can exhibit during such conditions. Figure 76 illustrates an example response for the `load_playback` component to a close-in three-phase fault.

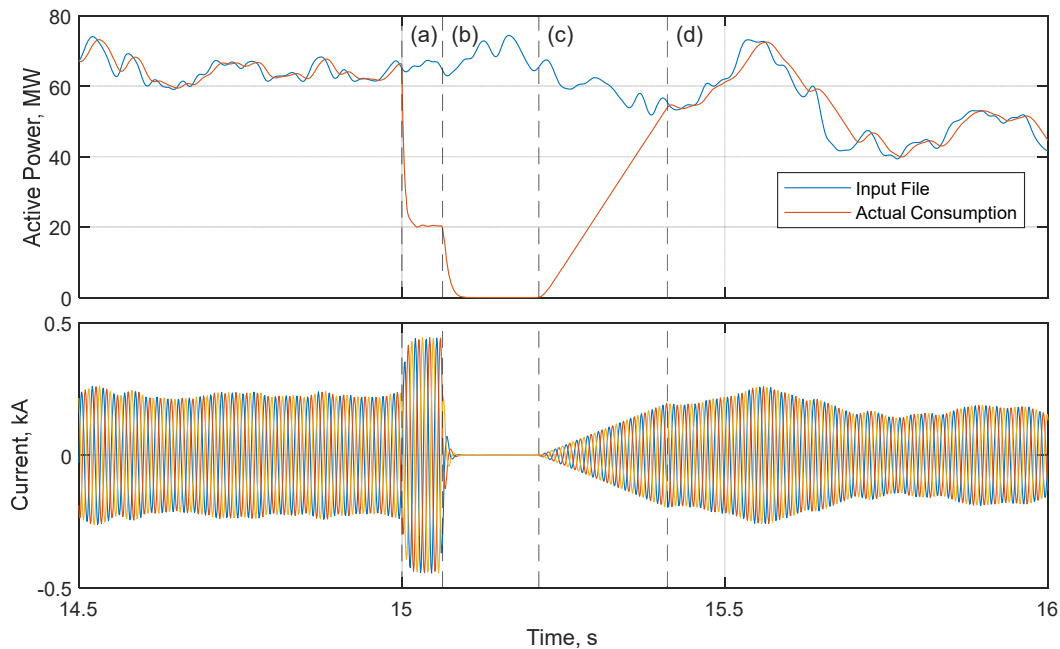


Figure 76: Exemplar Response of `load_playback` Component to Close-In 3 PH Fault Initiated at $t = 15$ s and Cleared at $t = 15.1$ s. Active Power Consumption Dips at Time (a) as the Load Current is Maintained within the Specified Limit of Roughly 400 A. At Time (b), the `load_playback` Component Enters Momentary Cessation and at Time (c), which is Shortly After the Fault is Cleared, Exits Momentary Cessation. The Ramp Rate of the Returning Load Current is Also Limited and Ramping Terminates at Time (d).

Observe that the fault does not halt or pause playback of the input file (i.e., it is assumed that the site-level process is continuing and supported by some on-site energy storage). Additionally, the post-undervoltage ramp-rate limiting affects the current limits rather than the current itself, meaning that the load will return to normal operation more quickly if it is operating at less than rated load.

Table 36: Input Parameters for `load_playback` Component.

Name	Units	Use
Nominal Active Power	MW	Defines nominal active power base.
Nominal Voltage	kV L-L RMS	Defines nominal voltage base.
Nominal Frequency	Hz	Defines nominal frequency base.
Current Limit	pu	Define current limit during voltage sags. A value of 1.25 is reasonable for most electronics with ride-through capability.
Current Source Time Constant	s	First-order low-pass filter to approximate response of electronic controls. A value of 2 to 10 ms is reasonable.
Enable UV Cessation?	Boolean	If nonzero, the load current will be regulated to zero in response to undervoltages below a set threshold for a set time delay.
UV Cessation Pickup	pu	Voltage magnitude threshold for entering UV cessation. Operates based on the lowest RMS L-G voltage magnitude.
UV Cessation Pickup Time Delay	s	Voltage magnitude must be below UV Cessation Pickup for this time duration for the load to enter UV Cessation.
UV Cessation Dropout Time Delay	s	For UV cessation to end, the voltage magnitude must exceed the UV Cessation Pickup for this time duration.
Post-UV Reconnection Ramp Time	s	Time over which current limits are ramped from 0 to rated limits after UV cessation has ended. If load current is less than the current limit, the time to return to normal operation will be reduced proportionally. For example, assume the current limit is 1.2 pu and the Post-UV Reconnection Ramp Time is 2 seconds. If the normal load current at this time is 0.4 pu, it will take the load $(0.4 / 1.2) \times 2 = 0.667$ s to return to normal operation.

7.16 Lumped LV Cable, 1 PH – `LV_cable_1PH`

See `LV_cable_3PH`. This component exists because PSCAD does not allow the dimensions of nodes on modules to vary dynamically. This model differs from `LV_cable_3PH` only in that the electrical nodes on this component have a dimension 1, instead of 3.

7.17 Lumped LV Cable, 3 PH – `LV_cable_3PH`

A lumped-parameter model for low-voltage cables, specifically meant for convenient (but relatively low-fidelity) representation of the low- and medium-voltage cables used in collection/distribution circuits in large industrial facilities or inverter-based generation plants. When performing EMT studies of such applications, it is often necessary to have some

thoughtfully-placed resistances to damp unrealistic and spurious transients, but it can be time consuming to place these. This model allows for some credible damping to be added without the large input data burden associated with a more formal cable constants routine.

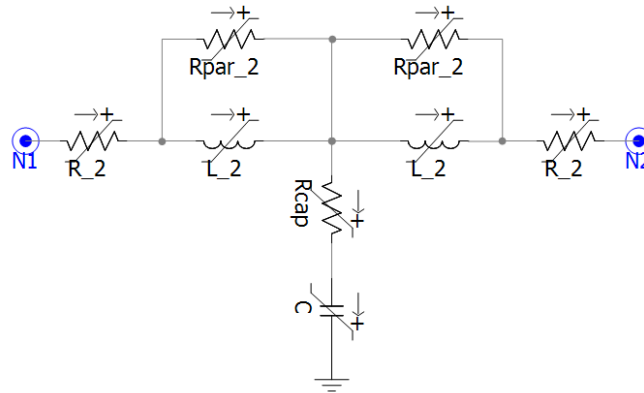


Figure 77: Topology of LV_cable_3PH.

A T-circuit is used instead of a π -circuit to ensure there is at least some inductance present in the same mesh as the capacitive current whenever the capacitor is suddenly discharged (e.g., due to a fault). A parallel damping resistance (R_{par}) and series shunt resistance (R_{cap}) are used to approximate the frequency dependent losses of the cable, providing some attenuation of high-frequency switching noise and/or numerical oscillations.

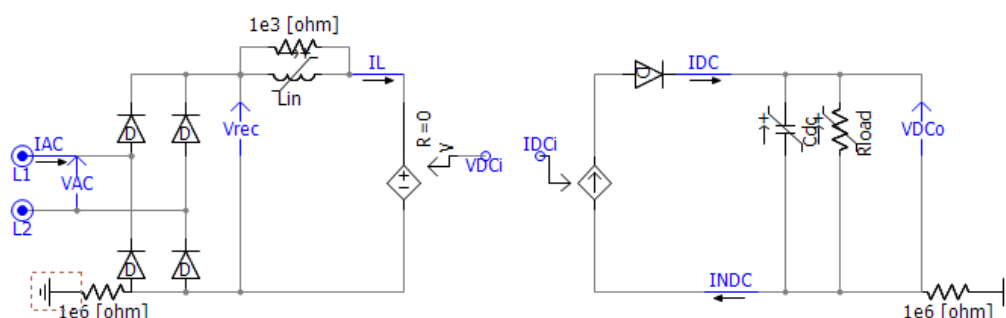
The LV_cable_3PH component provides no representation of zero-sequence coupling—the underlying assumption is that this cable model is being used for grid-level studies wherein the zero-sequence networks of the data center and the grid are isolated from one another via delta-wye transformers.

Table 37: Input Parameters for LV_cable_3PH Component.

Name	Units	Use
Resistance	$\Omega/1000$ ft	N/A
Inductance	H/1000 ft	N/A
Avg. Length	ft	Assumed length of a single circuit
No. of Parallel Circuits	N/A	Series inductance, resistance is decreased proportionally to this value while shunt capacitance is increased proportionally.
Propagation Speed	Fraction of speed of light	Capacitance is estimated based on inductance and lossless transmission line equation. Usually in the range of 0.8 to 0.9 for low-voltage cables—this value does not include reduction in propagation speed from series resistance.
Cutoff Frequency, Hz	Hz	Frequency at which parallel damping resistance is equal to magnitude of impedance from series inductance.

7.18 1 PH Rectifier with PFC, AVM – pfc_avm

The `pfc_avm` component is a variation of the `pfc_swm` component that uses an AVM. The IGBT of the boost converter is replaced with controlled current and voltage sources. A timestep of 50 μ s or less is recommended. For grid-level studies, users are encouraged to use this AVM variant instead of the SWM.

Figure 78: Main Hardware Schematic for `pfc_avm`.

The input parameters for `pfc_avm` are the same as those for `pfc_swm` (see), with the exception that the carrier frequency is absent as there is no PWM represented in `pfc_avm`.

Note that, as the `pfc_avm` component contains a built-in load but no built-in energy storage, activation of the momentary cessation function will usually cause rapid DC link voltage collapse unless a DC-DC converter with energy storage is connected to the DC link. See the system models DML_DC_Dist_UPS or DML_PFC_Demo or examples of how to do this.

Table 38: Device Rating Parameters for `pfc_avm` Component.

Name	Units	Use
Nominal Power Consumption	MW	Defines power consumption of Rload at nominal voltage
Nominal AC Voltage	kV RMS	DC link voltage is assumed to be 1.6 times this value
Loading level	pu	Active power consumption of the DC side resistive load. A variable input signal may be used to simulate varying load profiles.
AC Current Limit	pu	Limit for scaling-based current limiter. Note this control cannot suppress all transient overcurrents and overcurrent tripping for faults is still possible, especially for close-in or long-lasting faults.
DC Link Capacitance, μF	μF	N/A
Boost Converter Inductance	H	N/A
Model Startup Time	s	Protection functions are disabled until simulation time exceeds this value.

Table 39: Controller Setting Parameters for `pfc_avm` Component.

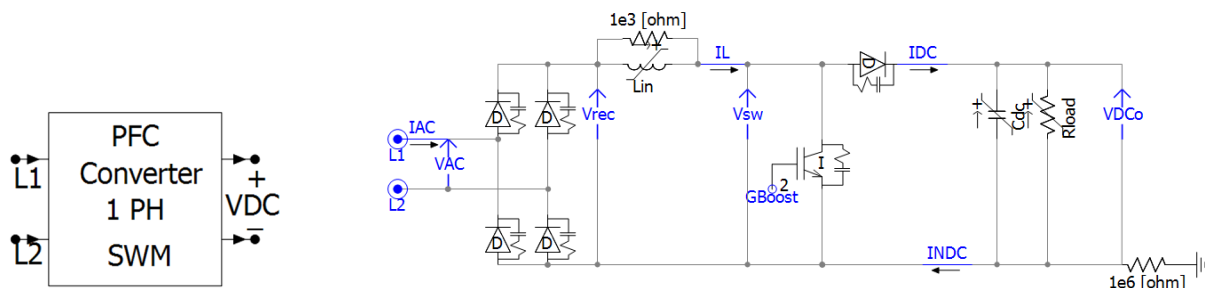
Name	Units	Use
Measurement Time Constant	s	First-order low pass filter applied to voltage, current measurements used in control loops.
Volt. Reg., Prop Gain	A/V^2	DC voltage regulator (outer) control loop, determines amplitude of current reference
Volt. Reg., Int. Time Constant	$A/V^2\cdot s$	
Curr. Reg., Prop Gain	1/A	Inductor current regulator (inner) control loop, determines modulation index.
Enable Momentary Cessation?	Boolean	If nonzero, voltage sags will cause the current to be regulated to zero for the duration of the sag.
Voltage Sag Threshold	pu	Magnitude threshold below which a voltage sag is declared. Operates based on RMS input voltage.
Momentary Cess. Pickup Time Delay	s	Time duration for which voltage sag must persist to trigger start momentary cessation
Momentary Cess. Dropout Time Delay	s	Time duration for which voltage must be above the minimum reconnection voltage to trigger end of momentary cessation.
Mom. Cess., Walk-In Time	s	After momentary cessation ends, the current limit will be gradually ramped from 0 to 1 (and onwards to the user-specified limit). The time required for the component to return to the pre-cessation current is equal to this time multiplied by the loading level. For example, a walk-in time of 5 s and loading level of 50% corresponds to a 2.5 s recovery time.
Mom. Cess., Min. Recon. Voltage	pu	AC voltage must be above this threshold for the set dropout time delay in order to trigger end of momentary cessation.

Table 40: Protection Setting Parameters for `pfc_avm` Component.

Name	Units	Use
Enable DC Undervoltage trip?	Boolean	N/A
DC Undervolt., Voltage Thresh.	pu	DC link undervoltage element, trips PFC front-end if measured voltage drops below set threshold for set time period.
DC Undervolt., Pickup Time Delay	s	
Enable DC Overvoltage trip?	Boolean	N/A
DC Overvolt., Voltage Thresh.	pu	DC link overvoltage element, trips PFC front-end if measured voltage drops below set threshold for set time period.
DC Overvolt., Pickup Time Delay	s	
Enable Overcurrent trip?	Boolean	N/A
Overcurrent, Current Thresh.	pu	AC overcurrent element, trips PFC front-end if measured voltage drops below set threshold for set time period.
Overcurrent, Pickup Time Delay	s	

7.19 1 PH Rectifier with PFC, SWM – `pfc_swm`

The `pfc_swm` component is a single-phase switched mode power supply with a full bridge diode front-end and DC/DC boost converter which provides (distortion) power factor correction. While previously used specifically to replicate the grid dynamics of cryptocurrency mining hardware [61], the design's major elements are commonly used in single phase power supplies for electronics. In the DML examples, it is used to represent small electronic loads.


 Figure 79: Icon (Left) and Main Hardware Schematic (Right) for `pfc_swm`.

The `pfc_swm` requires a high switching frequency (e.g., many tens of kilohertz) to function properly. A timestep of 1 μ s or less should be used—users are encouraged to use the AVM

variant (`pfc_avm`) for grid-level studies. The purpose of developing this SWM was to verify the sufficiency of the AVM.

The PFC control varies the duty cycle of GBoost to maintain V_{DCo} at a constant reference. An intermediate current regulator is also used to regulate I_L to be a rectified sine wave. This is the power factor correction stage—its effect is to make I_{AC} roughly sinusoidal, instead of the distorted waveform associated with a simple diode rectifier. This is the primary feature that causes the grid-level behavior of the PFC converter to differ so significantly from that of a basic diode rectifier (e.g., of the type used in `rect_3x_full_wave`).

In a real power supply, there are additional converters and electronics downstream to further condition the voltage for the electronics. For grid-level studies, these are reduced simply to R_{load} , which can be varied to simulate varying compute workloads.

The input parameters for `pfc_swm` are identical to those for `pfc_avm` (Table 38, Table 39, and Table 40).

7.20 PI Controller with Anti-Windup Logic – `PI_AntiWindUp`

The `PI_AntiWindUp` component is a simple modification of the basic PI controller to include two additional functions to avoid unwanted windup of the integrator:

- 1) When freeze signal, `frz`, is nonzero, the input to the proportional gain is held at the previous value and the input to the integrator is set equal to 0.
- 2) The difference between the integrator output and user-set controller limit is fed back to the integrator, ensuring that the integrator value is frozen when it hits the limits.

This component is very similar to a user-defined module commonly included in PSCAD's built-in example files (but not the base component library).

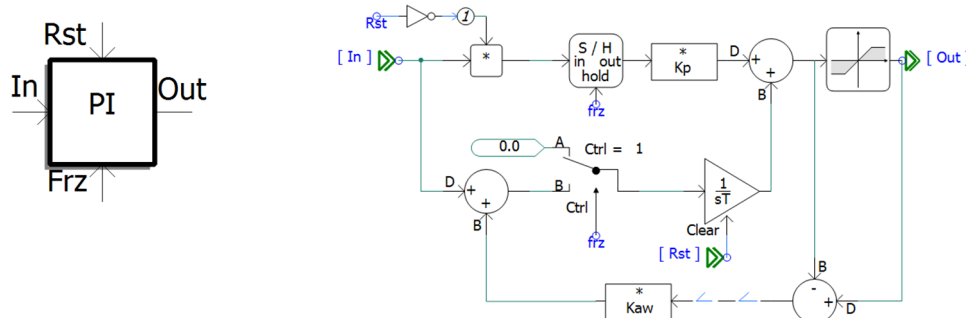


Figure 80: Icon (Left) and Main Control Diagram (Right) for `PI_AntiWindUp` Component.

Table 41: Input Parameters for PI_AntiWindUp Component.

Name	Units	Use
Maximum output limit	N/A	N/A
Minimum output limit	N/A	N/A
Proportional gain Kp	N/A	N/A
Integrator time constant	s	N/A
Anti wind-up gain	N/A	A value of 1 is desired in most cases and results in total elimination of windup when limits are hit.

7.21 dq-Domain Power Calculation – PQ_dq

The PQ_dq component implements the dq-domain equations for instantaneous real and reactive power. It can also convert the outputs to per-unit and filter them using a first order low-pass filter. The component's purpose is to increase the organization and readability of schematics.

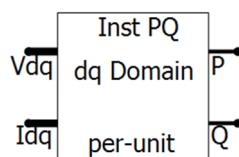


Figure 81: Icon for the PQ_dq Component.

Table 42: Input Parameters for PQ_dq Component.

Name	Units	Use
Filtering time constant	s	First-order low-pass filter on power calculations
Power base	MVA	Defines apparent power base. Set equal to 1 if inputs are already in per unit.

7.22 Per-unit Base Calculator – pu_bases

The pu_bases component computes base values (impedance, time, etc.) that are implicitly defined once one has defined a voltage, power, and frequency base. The component's purpose is to improve the organization of schematics and reduce time spent troubleshooting scaling and/or per-unitization issues.

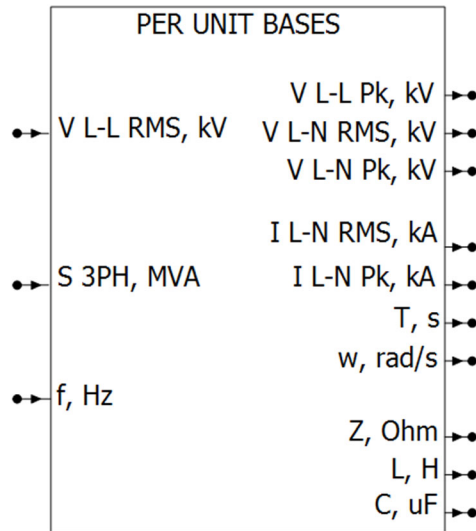


Figure 82: Icon for the `pu_bases` Component.

This component has no input parameters. The user supplies the voltage base (in kV L-L RMS), three-phase apparent power base (in MVA), and frequency base (in Hz)—all remaining bases may be derived from these. The units of output bases are shown on Figure 82 and are the default units used by PSCAD.

7.23 3 PH Set of 1 PH Rectifiers – `rect_3x_full_wave`

The `rect_3x_full_wave` component implements a 3 PH set of single-phase full-bridge diode rectifier loads. The rectifiers are connected line-to-line. For data center models, this component provides a simplified aggregate representation of small drive-supplied motor loads (e.g., centrifugal fans for CRAH). A series reactor, sized on a per-unit basis, is included. Small variations in load balancing are supported, but the user should manually override the capacitor values (which are balanced) if simulating large differences in the actual capacity of drives connected to a given phase.

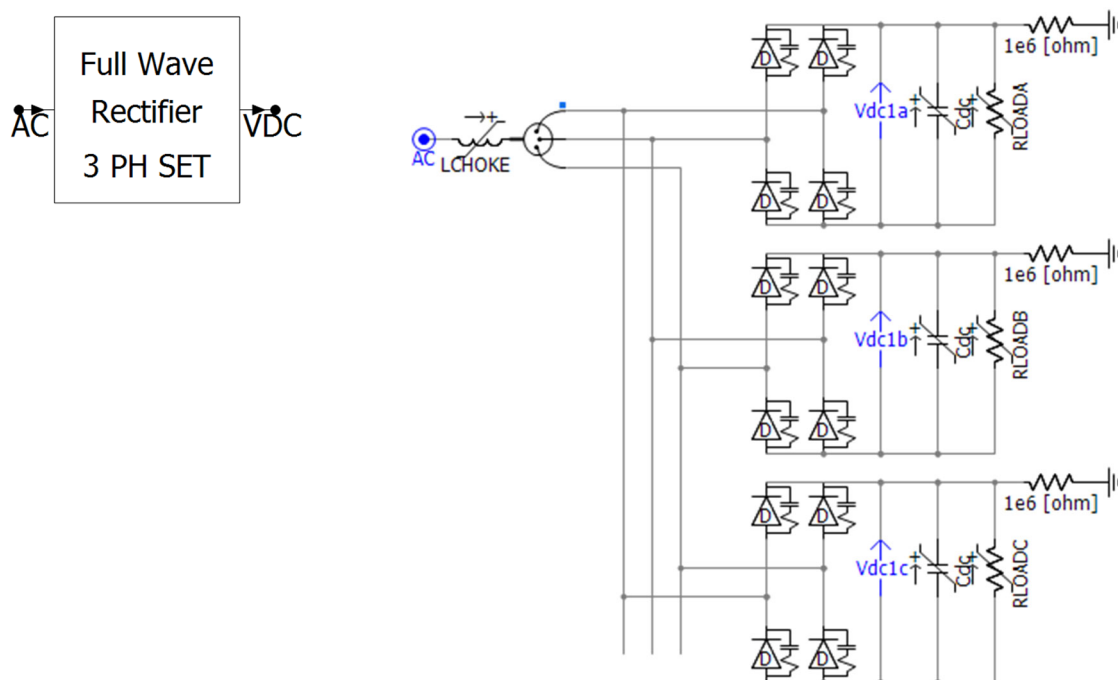


Figure 83: Icon (Left) and Electrical Schematic (Right) for `rect_3x_full_wave` Component.

Table 43 describes the input parameters for the `rect_3x_full_wave` component. To avoid needing to resize passive components, it is recommended to implement alternate power and voltage ratings using PSCAD's built in scaling components.

Table 43: Input Parameters for `rect_3x_full_wave` Component.

Name	Units	Use
Nominal Power Consumption	MW	Based on DC side consumption—apparent power flow from harmonics not included.
Nominal L-L AC Voltage	kV RMS	Defines voltage base.
Nominal AC frequency	Hz	Defines frequency base.
Per-phase DC Link Capacitance	μF	N/A
AC Side Inductance	pu	Series reactors are commonly added to protect drives from inrush current, transient overvoltages. A value of 0.03 to 0.05 pu is typical.
Overall loading level	pu	Actual three phase power consumption as a fraction of nominal power consumption.
Fraction of Load on AB Phases	pu	Value between 0 and 1, 0.333 typical. The fraction on CA is obtained by subtracting AB and BC fractions from one.
Fraction of Load on BC Phases	pu	

7.24 3 PH Set of 1 PH Rectifiers with Protection – `rect_3x_full_wave_c`

The `rect_3x_full_wave_c` component is identical to the `rect_3x_full_wave` component except in that it includes a set of single-phase contactors (`uv_sw_1PH`) which allows the component to represent per-phase tripping of small motor drives. This model introduces no new functionality over the `rect_3x_full_wave` and `uv_sw_1PH` components and is included primarily for convenience.

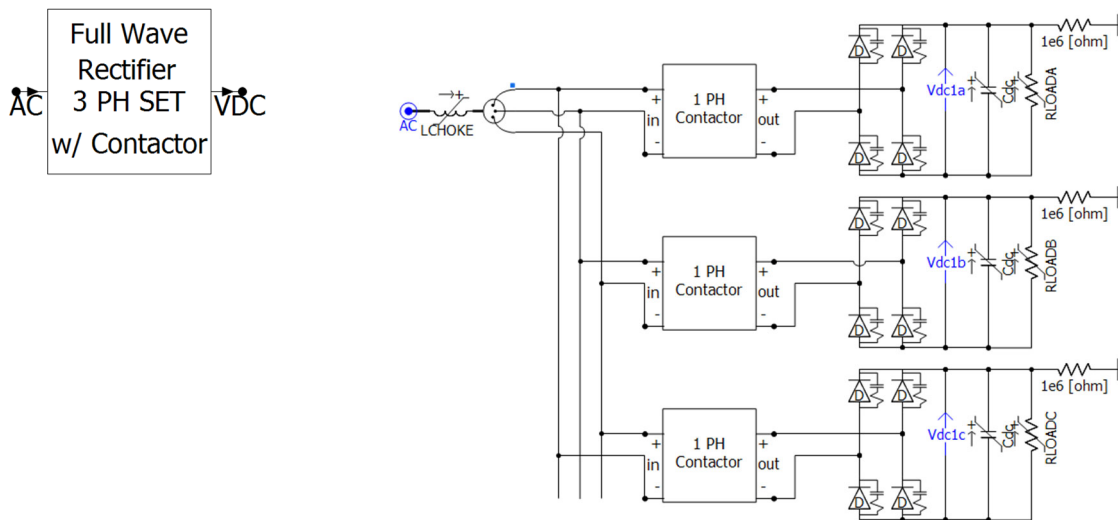


Figure 84: Icon (Left) and Electrical Schematic (Right) for `rect_3x_full_wave_c` Component.

Refer to the input tables for `rect_3x_full_wave` (Table 43) and `uv_sw_1PH` (Table 50) for explanations of the input parameters for this component.

7.25 3 PH Diode Rectifier – `rect_six_pulse`

The `rect_six_pulse` component implements a three-phase six-pulse rectifier. For data center models, this component provides a simplified aggregate representation of large drive-supplied motor loads (e.g., pumps for the chilled water plant). A series reactor, sized on a per-unit basis, is included.

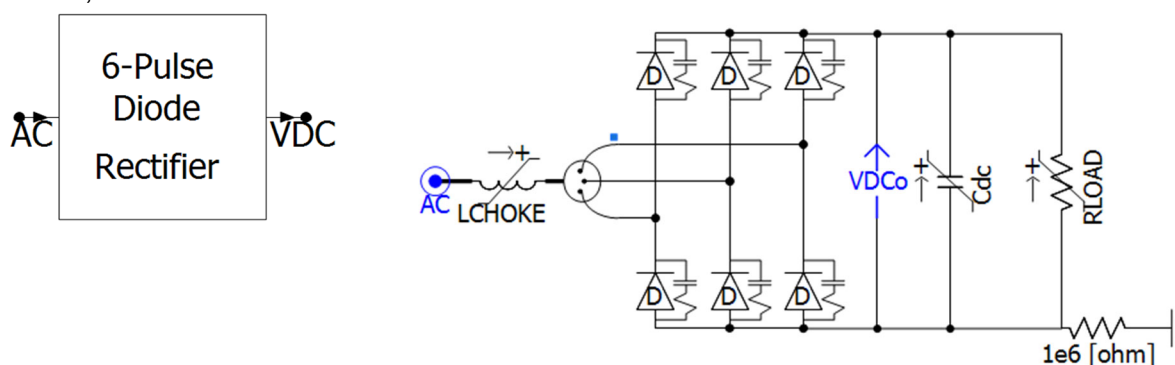


Figure 85: Icon (Left) and Electrical Schematic (Right) for `rect_six_pulse` Component.

Table 44: Input Parameters for `rect_six_pulse` Component.

Name	Units	Use
Nominal Power Consumption	MW	Based on DC side consumption—apparent power from harmonics not included.
Nominal L-L AC Voltage	kV RMS	Defines voltage base.
Nominal AC frequency	Hz	Defines frequency base.
Per-unit Load	pu	DC-link loading as a fraction of nominal power consumption.
Per-phase DC Link Capacitance	μF	N/A
AC Side Inductance	pu	Series reactors are commonly added to protect drives from inrush current, transient overvoltages. A value of 0.03 to 0.05 pu is typical.

7.26 Stabilizer for Droop-Based GFM Control – `stage2_ilm`

The `stage2_ilm` component implements a supplementary current limiting control for droop-based GFM inverters [104]. It is used as an optional feature in the `gfm_ibr_droop_swm` and `gfm_ibr_droop_avm` inverter models.

A major benefit of this control is enhancing the stability of the droop control during faults; the basic droop control (`gfm_droop`) is susceptible to losing synchronism during faults as it cannot output sufficient real power. The `stage2_ilm` control accomplishes this (along with current limiting) by reducing the real and reactive power references based on the d - and q -axis overcurrents, respectively:

There are no input parameters for the `stage2_ilm` component, as it is not anticipated that DML users will often need to adjust this model's parameters.

7.27 Unbalance Calculation – `unb_rms`

The `unb_rms` component computes voltage unbalance from a set of 3 voltage magnitudes in accordance with ANSI 47, which is commonly applied to protective relays and contactors used in industrial power systems. The input and output signals are in per unit.

7.28 UPS Controller – `ups_ctrl`

The `ups_ctrl` component is used for double conversion UPS modeling and is responsible for protection functions and the transferring of the UPS between different operating modes. Three operating modes are supported: normal, bypass, and battery. These are illustrated in Figure 86 and Table 45.

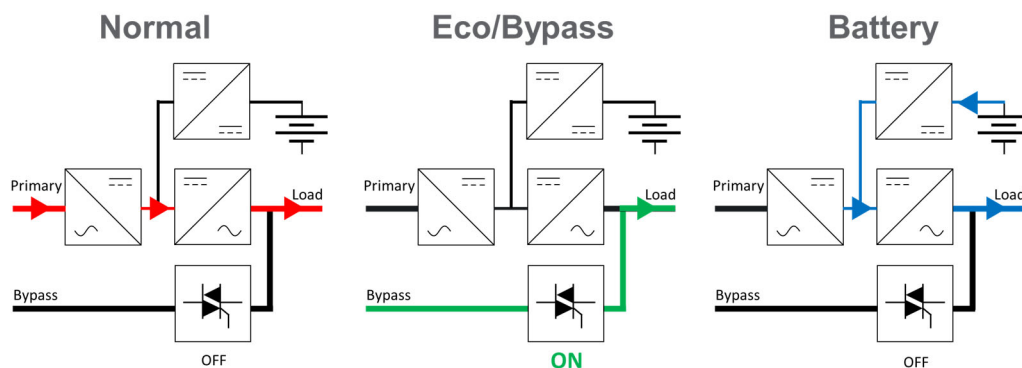


Figure 86: UPS Operating Modes and Corresponding Power Flow Paths [105].

Table 45: Correspondence of UPS Controller Operating Modes to Rectifier/Bypass Status.

Operating Mode	Rectifier Status ¹	Bypass Status
Normal ²	On	Open
Bypass	Off	Closed
Battery	Off	Open

¹This corresponds to the blocking of the rectifier IGBTs, not the opening of a mechanical switch.

²More properly, this is “double conversion” mode—the term “normal” may be more intuitive for users less familiar with UPS who need to configure the model.

Two sets of voltage-based protection functions are supported—one for the bypass mode and another for normal mode. The bypass mode protections are intended to be set far more sensitively, as the downstream load is directly connected to the grid in bypass mode. Bypass protections trip only the bypass and rectifier protections trip only the rectifier. For example, if the UPS is operating in bypass mode and the bypass protections trip, the UPS will transition to normal mode—the rectifier will remain online until the rectifier protections trip. If the rectifier protection trips as well, the rectifier will turn off as well, and the UPS will be operating in battery mode.

The `ups_ctrl` component supports auto-reconnection for the rectifier (but not the bypass) following a protection trip, but there is no synchronization or soft-start type features integrated. To simulate ramped UPS reconnection following a voltage sag, it is better to use the momentary cessation in the rectifier model (`gfl_ibr`). Future versions may include additional synchronization logic for the UPS output inverter (which needs to be synchronized with the grid side voltage prior to closing the bypass switch) so transitions to bypass mode can be simulated.

The `ups_ctrl` component does not handle LVRT functionality (i.e., rectifier controls that respond to sags in grid voltage), its only output capability is to switch the bypass and/or rectifier on or off. LVRT functions such as momentary cessation and dynamic voltage support are implemented in the rectifier (`gfl_ibr`).

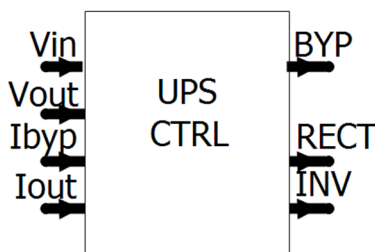
Figure 87: Icon for the `ups_ctrl` Component.

Table 46, Table 47, and Table 48 describe the parameters used to configure the `ups_ctrl` component.

Table 46: Rating-Related Parameters for `ups_ctrl` Component.

Name	Units	Use
Nominal AC Voltage	kV L-L RMS	Defines voltage base for voltage-related protections.
Nominal Apparent Power	MVA	Defines apparent power base; not presently used.
Nominal AC Frequency	Hz	Defines frequency base; not presently used.
Initial Operating Mode	N/A	Choose one of the options described in Figure 86; Normal is the most typical state for data center UPS.
Startup Time	s	Protection functions are blocked from operating until simulation time exceeds this value.

Table 47: Bypass Control-Related Parameters for `ups_ctrl` Component.

Name	Units	Use
Enable AC bypass undervoltage	Boolean	Phase undervoltage protection element: will open the bypass switch if the grid AC voltage magnitude drops below the pickup value for the set time delay.
Bypass undervoltage pickup	pu	
Bypass undervoltage time delay	s	
Enable bypass volt. unbalance?	Boolean	Phase voltage unbalance element (ANSI 47 definition); will open the bypass switch if the grid AC voltage unbalance exceeds the pickup value for the set time delay.
Bypass volt. unbalance pickup	pu	
Bypass volt. unbalance time delay	s	
Enable AC bypass overvoltage?	Boolean	Phase overvoltage protection element: will open the bypass switch if the grid AC voltage magnitude exceeds the pickup value for the set time delay.
Bypass volt. unbalance pickup	pu	
Bypass overvoltage time delay	s	

Table 48: Rectifier Protection-Related Parameters for `ups_ctrl` Component.

Name	Units	Use
Enable AC bypass undervoltage	Boolean	Undervoltage protection element: will turn off rectifier if the grid AC voltage magnitude drops below the pickup value for the set time delay.
Bypass undervoltage pickup	pu	
Bypass undervoltage time delay	s	
Enable bypass volt. unbalance?	Boolean	Voltage unbalance element (ANSI 47 definition); will turn off rectifier if the grid AC voltage unbalance exceeds the pickup value for the set time delay.
Bypass volt. unbalance pickup	pu	
Bypass volt. unbalance time delay	s	
Enable AC bypass overvoltage?	Boolean	Overvoltage protection element: will turn off rectifier if the grid AC voltage magnitude exceeds the pickup value for the set time delay.
Bypass volt. unbalance pickup	pu	
Bypass overvoltage time delay	s	
Enable auto-reconnection?	Boolean	If nonzero, the rectifier will turn back on after the set time delay so long as the undervoltage, overvoltage, or unbalance protections are not timing.
Auto-Reconnection Time Delay	s	

7.29 3 PH Contactor – `uv_sw`

The `uv_sw` component represents a three-pole, three-phase contactor with undervoltage and voltage unbalance protections, is commonly used to ensure proper de-energization and restart of industrial processes (e.g., cooling) in response to voltage sags and/or significant voltage unbalance.

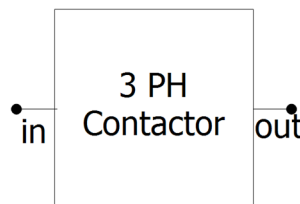
Figure 88: Icon for the `uv_sw` Component.

Table 49: Input Parameters for `uv_sw` Component.

Name	Units	Use
Nominal AC voltage	L-L RMS	Defines line-to-line voltage base.
Protected Voltage	Boolean	Select 1 for line-to-neutral voltage, 0 for line-to-ground voltage.
Enable Voltage Unbalance Protection?	Boolean	N/A
Startup time	s	Protection is disabled until simulation time exceeds this value
Nominal frequency	Hz	Used for RMS calculation
Undervoltage trip, pickup threshold	pu	RMS undervoltage element, opens contactor if measured voltage drops below set threshold for set time period.
Undervoltage trip, pickup time	s	
Volt. Unbalance Trip, Pickup Thresh.	pu	Voltage unbalance element (ANSI 47 method): opens contactor if measured voltage unbalance exceeds set threshold for set time period.
Volt unbalance trip, pickup time	s	

7.30 1 PH Contactor – `uv_sw_1PH`

The `uv_sw_1PH` component represents a two-pole, single-phase contactor with an undervoltage dropout, such as is commonly used to ensure proper de-energization and restart of industrial processes (e.g., cooling) in response to voltage sags.

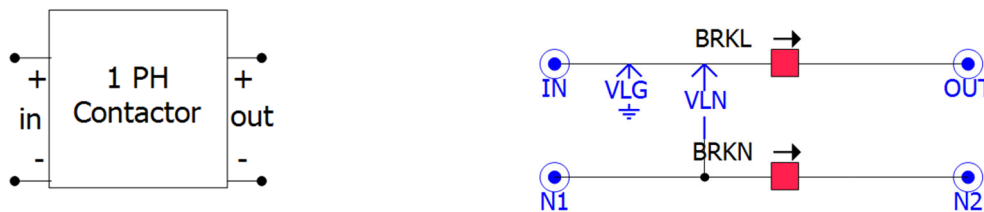
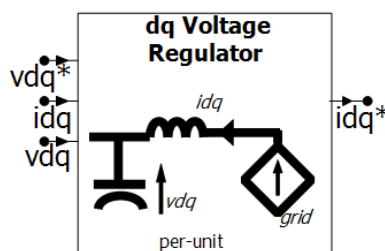

 Figure 89: Icon (Left) and Electrical Schematic (Right) for `uv_sw_1PH` Component.

Table 50: Input Parameters for `uv_sw_1PH` Component.

Name	Units	Use
Nominal AC voltage	RMS	Defines voltage base used for undervoltage protection
Protected Voltage	Boolean	Select 1 for line-to-neutral voltage, 0 for line-to-ground voltage.
Startup time	s	Protection is disabled until simulation time exceeds this value
Nominal frequency	Hz	Used for RMS calculation
Undervoltage trip, pickup threshold	pu	RMS undervoltage element, opens contactor if measured voltage drops below set threshold for set time period.
Undervoltage trip, pickup time	s	

7.31 dq-Domain Voltage Regulator – `v_reg`

The `v_reg` component determines the current reference necessary to track a given voltage reference. This control loop is often used in multi-layer GFM controls to convert the voltage reference from an outer control loop (e.g., `gfm_droop`) to a current reference for an inner control loop (e.g., `i_reg`).

Figure 90: Icon for `v_reg`.Table 51: Input Parameters for `i_req` Component.

Name	Units	Use
Kp, Voltage Regulator	pu	Proportional gain for PI controllers
Ti, Voltage Regulator	s	Integral time constant for PI controls
AC Side Capacitance	pu	Total shunt capacitance at node where <code>vdq</code> (see Figure 90) is measured.

7.32 Variable Frequency Drive, AVM – `vfd_avm`

The `vfd_avm` component represents a typical variable frequency drive for commonplace motor loads such as centrifugal pumps and fans. The front-end is six-pulse diode rectifier, the motor drive itself a three-phase VSC, and the motor is a squirrel cage induction motor designed for

efficiency, rather than for starting high torque loads. Figure 91 illustrates the central schematic of the `vfd_avm` model:

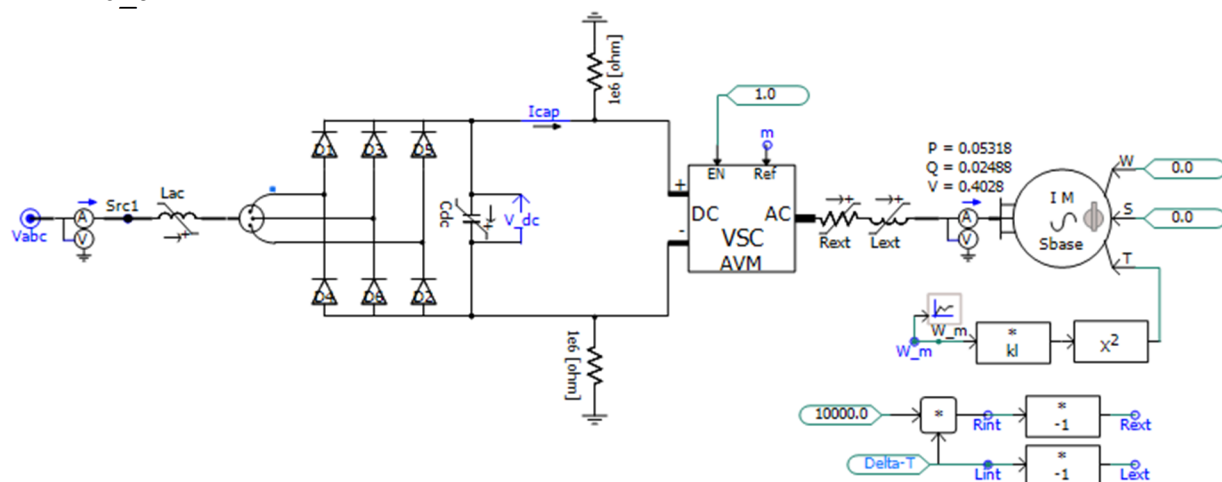


Figure 91: Central Schematic of the `vfd_avm` Model.

The mechanical load is assumed to be a fan or compressor and the mechanical torque applied to the motor increases with the square of the motor speed. The inverter uses an open-loop Volts/Hz speed control, which is widely used in such applications due to its simplicity and low cost. In the context of data center modeling, the `vfd_avm` model is meant to provide a more detailed representation of building-level cooling load than the comparatively simpler `rect_six_pulse` model, which represents the output inverter and motor simply as a resistance. The `vfd_avm` model is not well-suited for representing motor loads used in heavy industrial applications.

Table 52 lists the input parameters for the `vfd_avm` component.

Table 52: General input parameters for `vfd_avm` component.

Name	Units	Use
Motor rated voltage	kV L-N RMS	Nominal voltage of the motor. If this is greater than the AC voltage supplied to the VFD input, the motor may be unable to start or run at full speed.
Motor rated current	kV L-N RMS	Full load amps of the motor.
Relative drive rating	pu	Ratio of drive power rating to motor rating. A value of at least 1.5 is common, and lower values may cause the drive to have difficulty starting the motor.
Model startup time	s	Internal motor speed reference is set to one until this time. The speed control is rate limited and the motor will soft-start at this time (assuming the supplied speed reference is not nonzero).
AC side inductance	pu	Series inductance added to diode rectifier, a value of at least 0.03 pu is often used to protect the drive from inrush currents and transient overvoltages.
DC link capacitance	μ F	Capacitance present on the DC link. Recommended to select such that DC link ripple at full load is around 5%.
Enable output inverter I limit?	boolean	It is recommend to disable this only for troubleshooting. When disable, the ability of the drive to ride through disturbances is unrealistically improved.
Output inverter I limit	pu (on drive power base)	A value of 1.2 pu is typical. Defined in terms of drive rating, not motor rating.

Table 53: Protection input parameters for `vfd_avm` component.

Name	Units	Use
AC Overcurrent Pickup	pu (on drive power base)	Trips the output drive if any instantaneous phase current in the diode rectifier exceeds the pickup value for the set time delay. Per-unit value defined in terms of drive rating, not motor rating.
AC Overcurrent Time Delay	s	Time delay associated with AC Overcurrent pickup.
DC Overvoltage Pickup	pu	Trips the output drive if the DC link voltage exceeds the pickup value for the set time delay.
DC Overvoltage Time Delay	s	Time delay associated with DC Overvoltage pickup.
DC Undervoltage Pickup	pu	Trips the output drive if the DC link voltage falls below the pickup value for the set time delay.
DC Undervoltage Time Delay	s	Time delay associated with DC undervoltage pickup.

7.33 Variable Freq. Drive, AVM, 1 PH – `vfd_avm_1ph`

The `vfd_avm_1ph` component is identical to `vfd_avm` except in that it uses a full-bridge diode rectifier instead with a single-phase AC input rather than a six-pulse diode rectifier. Be aware that, for a given motor power rating, it is generally necessary to significantly increase the capacitance and drive capacity to a much greater value than that required for `vfd_avm`.

7.34 Variable Freq. Drive, SWM, 1 PH – `vfd_swm_1ph`

The `vfd_swm_1ph` component is identical to `vfd_swm` except in that it uses a full-bridge diode rectifier instead with a single-phase AC input rather than a six-pulse diode rectifier. Be aware that, for a given motor power rating, it is generally necessary to significantly increase the capacitance and drive capacity to a much greater value than that required for `vfd_swm`.

7.35 Variable Freq. Drive, SWM – `vfd_swm`

The `vfd_swm` component is a variation of `vfd_avm` that represents the output inverter using a two-level PWM-based inverter, rather than an AVM. It has the same input parameters.

8.0 References

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