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PNNL-35159

Understanding the Capabilities and Limitations of the Controls and Operations of High Voltage Direct Current (HVdc) Converters in Interconnected Electric Power Systems

September 2023

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U.S. DEPARTMENT OF ENERGY

Prepared for the U.S. Department of Energy
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Abstract

This project will seek to build a fundamental understanding, and capability, to model and simulate the controls and operations of high voltage direct current (HVdc) converter stations in an electromagnetic simulation environment. While HVdc stations have been operated in the United States for over 50 years, these are typically simple two terminal point-to-point systems. Recently multi-terminal systems have begun to be deployed. The challenge with these new multi-terminal systems is that they often use different control schemes on the different terminals. The interactions of existing and new controls, and the fact that HVdc systems are rates in the 1,000's of MWs means that small control instabilities can have dramatic impacts to bulk power systems. Despite these challenges, the operational capabilities of HVdc make them an attractive option for the transfer of the large amounts of renewable electricity that will be necessary for decarbonization of the nation's electrical infrastructure and other sectors.

Acknowledgments

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1.0 Introduction

1.1 Specific Aims

This project develops the modeling, simulation, and analysis capabilities needed to evaluate the impact of deploying muti-terminal HVdc systems. A fundamental understanding of these mixed control type systems is essential to evaluate the use of HVdc as a tool to enable decarbonization of the nation's electrical infrastructure and the electrification of other sectors. In addition to a review of fundamental control approaches, this project uses the hardware accelerated real-time simulation capabilities available using OPAL-RT equipment. Real-time simulators are the tool of choice for modeling complex control problems that must be run in real time. In this project, the OPAL-RT capabilities enable high-fidelity models of modular multi-level (MMC) HVdc converter stations in connection to HVac systems. An example of such a connection is shown in Fig. 1. This allows the development of use-cases that are directly applicable to DOE and industry. Using these capabilities and models, the goal is to fundamentally understand the implications of various individual converter control choices, their impact to the interconnected bulk power system, and how HVdc can best be used to support decarbonization and electrification goals.

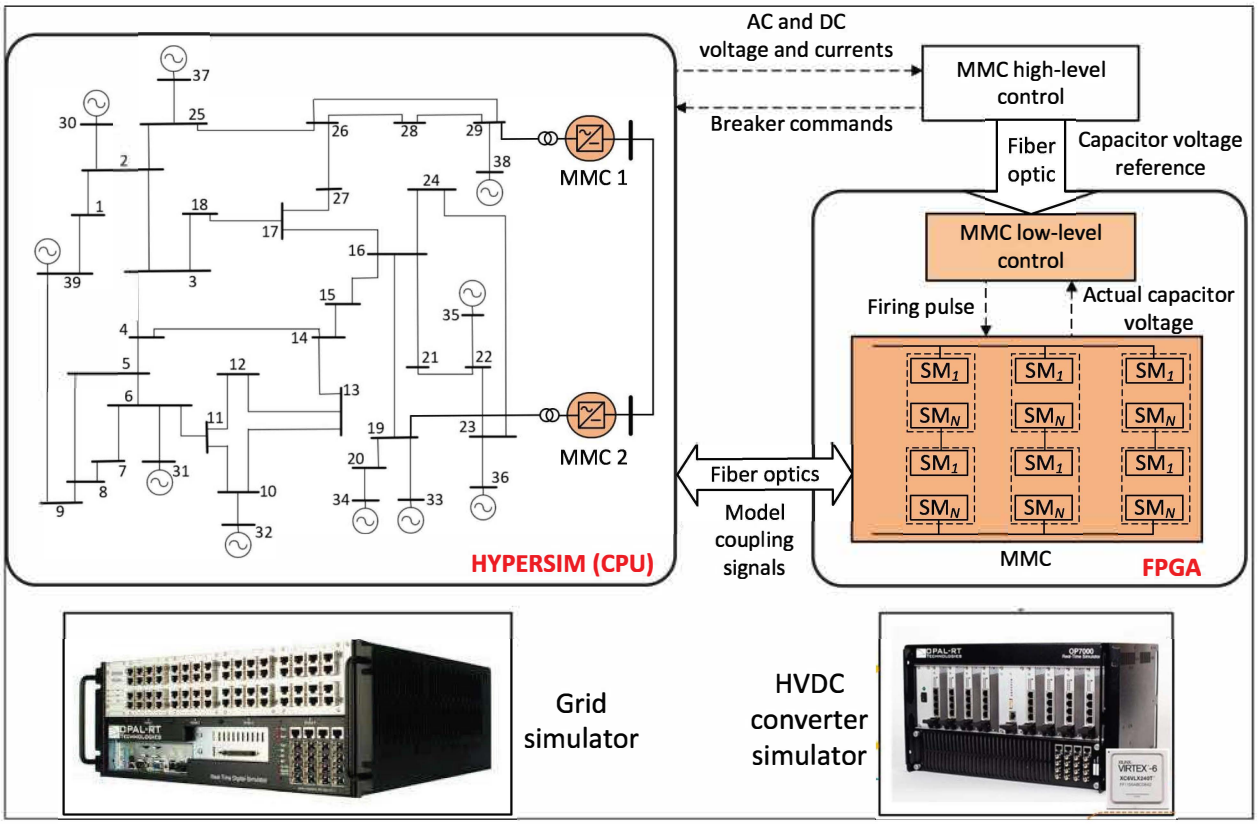

Figure 1. Example of how a 2-terminal HVdc system is emulated in connection to an existing a bulk HVac power system.

1.2 Background and Significance

Decarbonization of the nation's electrical infrastructure, and the associated electrification of end-use loads, requires a significantly higher transfers of electricity than are seen today. This is required because large scale renewable resources are not typically co-located with the load. Historically, transfers have been accomplished using the three synchronous electrical interconnects in the continental United States (Western, Eastern, and Texas). Increasingly high voltage AC, up to 765 kV, has been used to move power over long distances. However, interconnected AC systems require complex studies to increase the capability in any give line, because of the physics of AC circuits. Specifically, increasing the flow through a given line also affects the flows in parallel lines, with the result being that increasing the capacity of a single line may require the upgrading of multiple lines. Because of the power electronics converters of HVdc stations, it is possible to asynchronously transfer power over long distances. This was originally seen in the Pacific Coast Direct Current Intertie between Oregon and California which is rated at 3,800 MW. This facility pioneered much of the current understanding of how HVdc impacts bulk power systems, and they continue to deal with control issues because of the complexity and size of the system. The majority of HVdc lines in North America are simple point-to-point systems, but there is a recognized need for multi-terminal capabilities. This is especially true with variable output renewables where generation and line flow patterns can change continually. The deployment of multi-terminal HVdc systems increases the operational flexible of the bulk power system. In China, multiple HVdc lines have been built to transfer power from the West regions to the high density load areas of the east, and some of the newer systems are multi-terminal. In addition, a multi-terminal HVdc system increases the redundancy and thus system resilience in the case of one or a few of HVdc lines are out of service due to contingencies.

The fundamental challenge with multi-terminal HVdc systems is that it is possible to have different control systems on the different terminals. This is especially true in the United States where there are numerous utilities and any multi-terminal HVdc deployment is likely to be owned by multiple utilities. In this case, it is almost guarantees that the different terminals have different controls, if not completely vendors and technologies. In order to leverage HVdc to support decarbonization and electrification, it is essential to build modeling and simulation capabilities to understand the operational impact and interoperability capability of various control structures, and how they interact with the bulk AC system.

1.3 Research Design and Methodology

Given the short time frame of this effort, it leverages past work and knowledge to the greatest extent possible. This includes institutional capabilities in control theory, power electronics, and system level studies. The first step is to conduct an industry and literature review on the different types of controls that are used at individual HVdc converter stations, and how the controls are coordinated between stations. This is expected to include the well known voltage source and current source approaches, but the review includes variations in implementations to the greatest extent possible.

Based on the material found in the review, the project constructs a "simple" two-terminal HVdc system as part of a reduced order model of the Western Interconnect. This model will enable the various combinations of controls to be examines, identifying which approaches are better suited to coordinated operations. This includes internal converter station stability as well as the impact to the bulk power system. The key is to identify best practices and to develop the fundamental capabilities to be able to develop a future plan for analysis of multi-terminal deployments. Given the complexity of HVdc substation structure, fast converter-level control dynamics, and hundreds

of control signals exchanged between the HVdc switching components and controllers within each time step, we use PNNL's real-time hardware-in-the-loop simulation infrastructure to study the performance of different terminal controls and system-wide impacts of the HVdc system.

2.0 Literature Review

2.1 MMC Converter

Unlike most of existing MMC converter models in other platforms, either with control loop simplification in positive-sequence domain or equivalent arm's dc voltage in offline EMT domain, the studied model of MMC converter in this work is based on detailed modeling of a practical MMC converter. The detailed configuration of an MMC converter is shown in Fig. 2(a). It can be seen that each arm of the MMC converter consists of multiple submodules or cells, which can be half-bridge, full-bridge, and other configurations. The structure of a haft-bridge SM is shown in Fig. 2(b). Compared to other converter technologies, the advantages of MMC converters include:

- High-quality AC voltage generation [1]
- MMCs are highly modular in design. They can be scaled down or scaled up depending on the depending on the application requirement [2]
- Low di/dt and voltage stress on the insulation of the interfacing transformer
- No DC capacitor needed
- Low switching frequency of the individual SMs – reduced switching losses
- Due to the reduced harmonic content in the MMC output voltage, the need for extensive filtering requirements can be reduced
- Resilient to individual SM or the entire phase faults

On the other hand, the disadvantages of MMC converters include:

- Complex control and protection.

2.2 Substation-Level Control

Substation-level control refers to the control of entire or a subset of HVdc substations. In a multi-terminal HVdc system, the objectives of substation-level control include but not limited to:

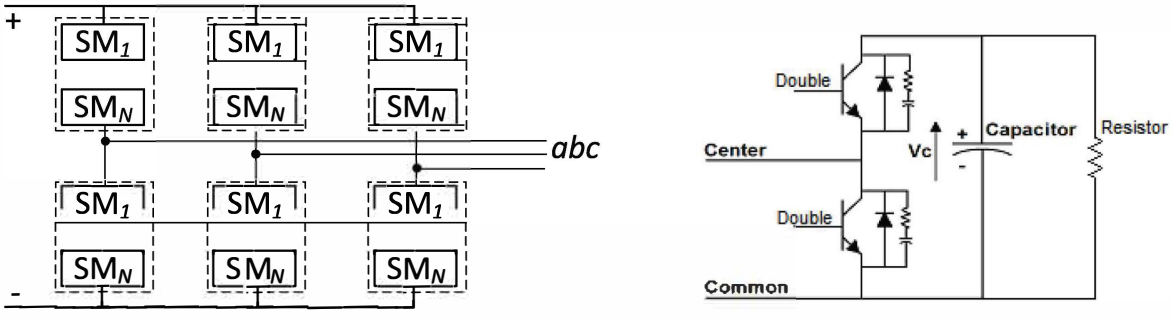

Figure 2. Structure of a) an MMC converter and b) a haft-bridge submodule configuration used in MMC arms.

- Achieve power sharing via $V_{dc} - P_{dc}$ droop to maintain HVdc system stability under different loading conditions [3–5].
- Provide grid services such as voltage and frequency support, congestion management, and inter-area oscillation damping to the HVac grid [6–8]
- Reduce system losses or operation cost by optimizing HVdc power flow and droop characteristics. [9, 10] .
- Protect HVdc system, including HVdc conerters, under short-circuit faults at the ac side and especially at the dc side.

In addition, the substation-level control can be realized by using centralized and decentralized approaches. In the former approach, one slack converter is responsible for regulating the HVdc grid voltage while the other converters operate in power control mode. Although the control of this approach is fairly simple, the entire multi-terminal HVdc system is vulnerable to a complete collapse once the slack converter fails.

Finally, substation-level control decides are used to translate operating modes of HVdc converters to mathematical equations when formulating and solving mathematical-based power flow and optimal power flow problems [3–5].

2.3 Converter-Level Control

Depending on the applications, the control objectives in the MMC converters can be classified into 4 types [1, 11, 12]:

- **Arm current control**: A basic approach to control the input and output currents and DC/AC voltages in the MMC converter is to control the current following through the arms. Depending on the application or the objectives of the MMC converters, the current following through the arms are regulated. The power flow control and the outer voltage controls considered in this study are implemented through the arm current control.
- **Circulating current control**: Due to the capacitor ripple voltages and multilevel modulation schemes, circulating currents are generated inside the MMC, which flow inside the MMC converter arms and do not go outside. To reduce the converter losses and improve controllability, circulating current controls are implemented for the MMC converters.
- **Capacitor voltage control**: The voltage controls are usually implemented to control the capacitor voltages at a predefined reference voltage level which is essential for the appropriate operation of the MMC converters.
- **Capacitor voltage balance control**: The capacitor voltage balance control is also widely presented in the literature which can be separated as the voltage balancing among the MMC arms and voltage balancing among the submodlues inside each arm.

2.4 HVdc Modeling Capability in HIL

Tables 1 and 2 summarizes the MMC-based HVdc modeling capability of OPAL-RT.

Table 1. Challenges of MMC modeling

Challenges	Opal-RT Solutions
Very small time step for SM	250 ns or 500 ns
Small time step for AC grid, arm inductors and transformer	20 to 60 micros using ARTEMIS-SSN or Hypersim nodal solver
Very small time step for arm inductor and transformer models	500 ns to 1 us using eHS FPGA nodal solver
Large number of SM per converter	1500 to 1800 cells per FPGA
Large number of terminals for HVDC grids	Use several FPGA boards
Connection to controller with fast rate and small latency	Aurora or Gigabit Ethernet 1 to 5 us update depending on number of optical fiber links and number of cells
Tested reliability	Several actual projects

Table 2. Put the table caption here

Each SM is individually simulated	yes
Each capacitor voltage is individually controlled	yes
Discrepancy of SM capacitance values	yes
Discharge resistance is simulated	yes
Resolution of firing signal	250 ns
Simulation of dead time	yes
Cell short circuit and other faults	yes
Forward voltage of diodes	yes
Diode non-linearity	no
Thermal effects due to switching loss of IGBT and diode turn-on and -off	not yet

3.0 System Modeling and Implementation in OPAL- RT

In this project, the system shown in Fig. 3 is implemented in a real-time co-simulation setup between HYPERsim and FPGA platforms of OPAL-RT. Key parameters of the system are shown in Table 3. Since developing grid-forming capability for either MMC2 or the wind plant is not in the scope of this project, a voltage source is needed at the offshore island to regulate the island voltage and frequency.

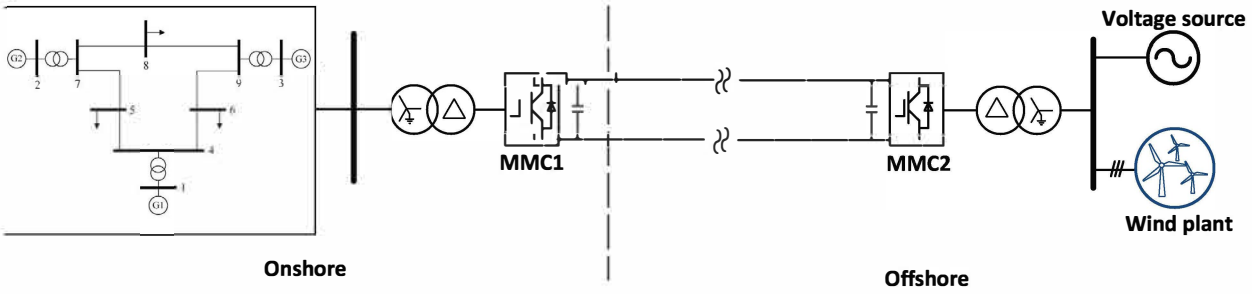

Figure 3. The configuration of an MMC-based 2-terminal HVdc transmission system connecting offshore wind to an onshore HVac bulk power system in the real-time simulation tool OPAL-RT.

Table 3. Parameters used in the test system.

Parameters	Values
Grid voltage and frequency at terminal 1	230 kV, 50 Hz
Grid voltage and frequency at terminal 2	230 kV, 50 Hz
Transformer at terminal 1	1400 MVA, 18/230 kV
Transformer at terminal 2	1400 MVA, 0.69/230kV
Rating of MMC1 and MMC2 converters	1000 MVA
Arm inductance and resistance of MMC1 and MMC2	0.04889 H, 0 Ω
HVdc voltage rating	580 kV
Wind power rating	32 MW

3.1 Multi-rate Modeling and Control of MMC-based HVdc Converters

In this work, a monopolar MMC-based HVdc transmission with haft-bridge configuration as shown in Fig. 2 is used. Key parameters of the 2-terminal MMC-based HVdc system are shown in Table 4.

As shown in Fig. 2, an MMC converter consists of a huge number of SMs. In addition, the simulation time step of MMC converters can be as low as 250-500 ns. Therefore, while the HVac and wind models in Fig. 3 are implemented in HYPERsim domain, the MMC converters with all SMs are modeled in FPGA. The multi-rate MMC modeling approach is shown in Fig. 4. In the FPGA side, detailed SMs of an MMC converter is simulated at HYPERsim. given the reference capacitor voltage and current each arm (valve) sent from the high-level controller in HYPERsim (CPU). It is important to note that the inner control loops in FPGA are associated with each individual SM voltage and current of an arm (valve). On the other hand, such a detailed

Table 4. Parameters of the 2-terminal HVdc system.

Parameters	Values
Number of SM per valve in MMC1	400
Number of SM per valve in MMC2	224
Voltage rating of each SM in MMC1	1.45 kV
Voltage rating of each SM in MMC2	2.59 kV
SM capacitance and resistance in MMC1	0.009 F, 2.2 kΩ
SM capacitance and resistance in MMC2	0.006 F, 2.2 kΩ
Carrier frequency	300 Hz
HYPERsim (CPU) time step	50 μs

MMC converter model in FPGA is modeled as an equivalent 3-phase voltage source converter in H-bridge configuration in HYPERsim. The operating point of this equivalent MMC converter in HYPERsim is characterized by the measured voltage and current of the entire corresponding arm (valve) in FPGA. Note that the equivalent MMC converter in HYPERsim is needed to establish explicit physical connections of the MMC converter to the HVac grid and wind farm models.

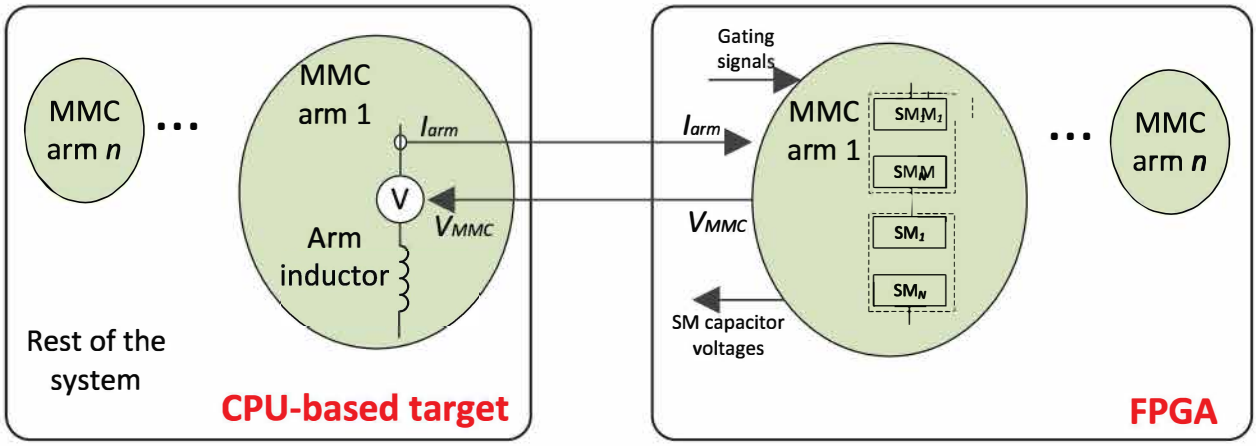

Figure 4. Multi-rate modeling approach of an MMC converter in HYPERsim and FPGA [12]

Regarding control, the control of an MMC converter includes a pole or high-level outer control loop and a valve-based or low-level inner control loop. The control objectives of the high-level and low-level control loops are shown in Fig. 8. As shown in Fig. 6, the high-level and low-level control loops are implemented in HYPERsim and FPGA, respectively. In the system in Fig. 3, assuming that MMC1 operates in P and Q model and MMC2 operates in Vdc and Q control mode, the inputs of the high-level control loop are the setpoints and actual measurements of the real and reactive power for MMC1 and MMC2. The outputs of the high-level control lop are the reference voltage and current for each converter arm (valve), which are sent to the low-level control loop in FPGA via I/O communication channels between the HYPERsim target and FPGA.

On the other hand, the inner valve-based or low-level control loop uses the reference values of arm voltages and currents to regulate the dc voltage and current of each SM (cell). In other words, these SMs are controlled individually. The output of the low-level control loop is the switching signals for switching devices of SMs. Details of the low-level control loop can be found in [13, 14]. As mentioned above, the measured voltage and current of each MMC arm are sent

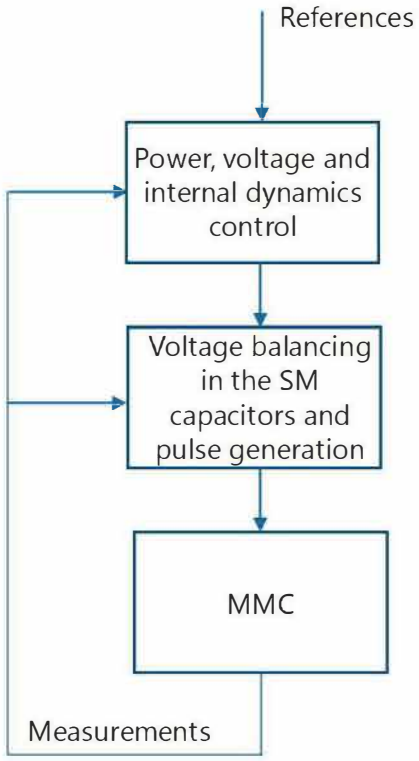

Figure 5. Control of MMC converters

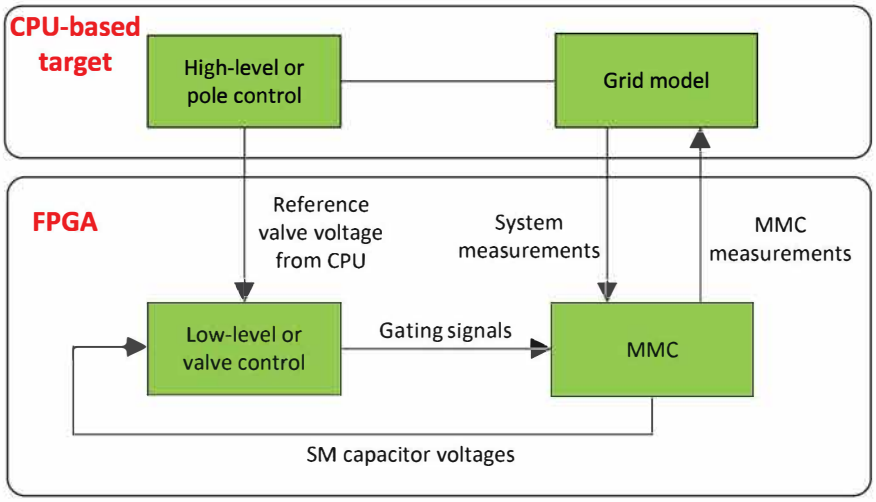

Figure 6. HIL structure of the MMC control in HYPERsim and FPGA.

back to the high-level control loop and the equivalent MMC converter model in HYPERsim (CPU). Although the instantaneous value of the valve voltages at the end of the previous CPU time step can be used, it is recommended to use the average valve voltage over the last CPU time step.

Fig. 8 shows the block diagram of the outer loop controller considered in this study which can be divided into four stages: active power P_{MMC} control, DC-bus voltage V_{dc} control, reactive power Q_{MMC} control, and AC-side voltage V_{ac} control. The active power and DC-bus voltage controls are respectively activated by turning on switches 1 and 2. The output of the switch is

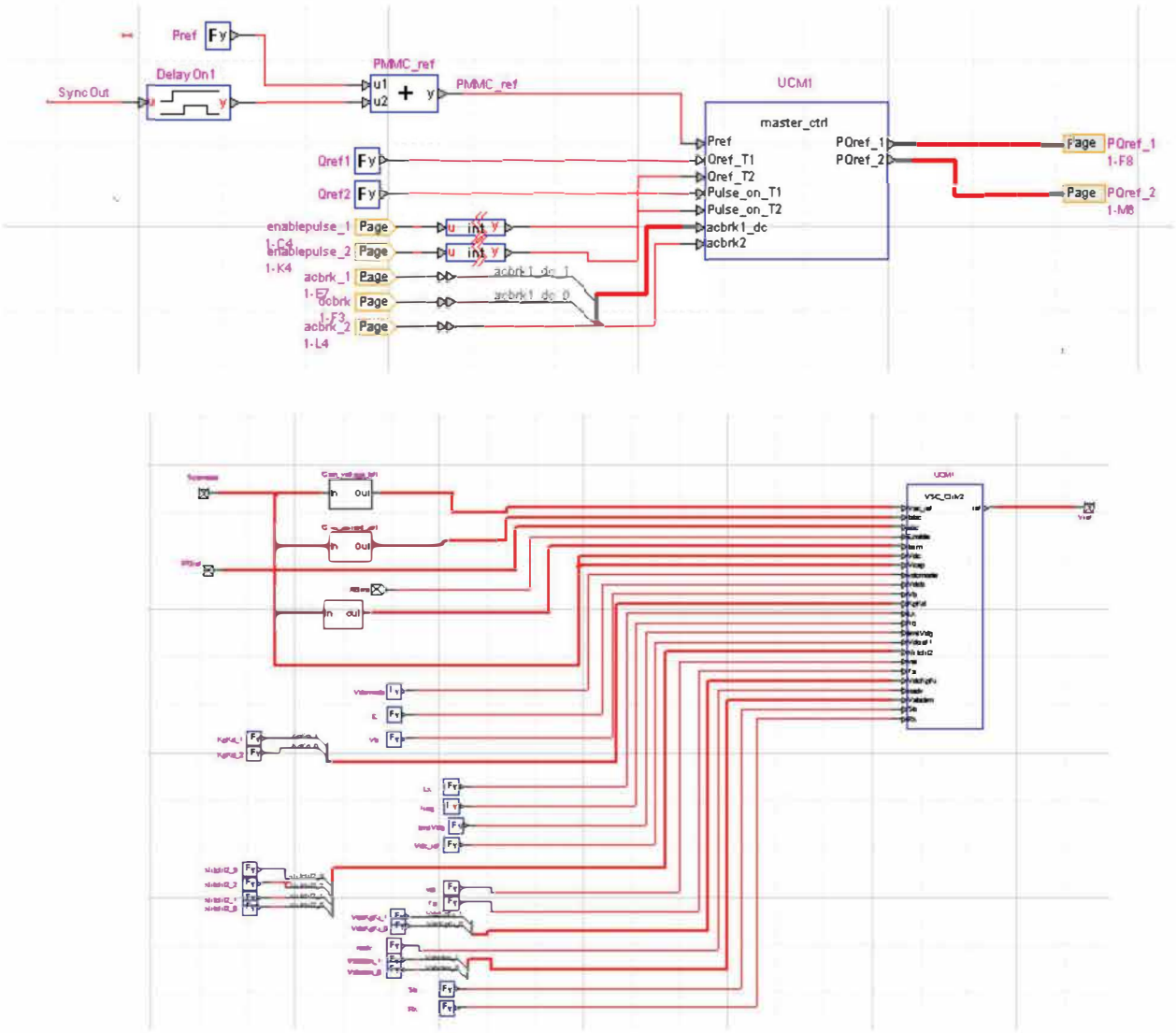

Figure 7. High-level control block in HYPERsim (CPU).

fed into a PI controller to generate the active current reference i_d^{ref} which is then compared with measured active current i_d. Finally, the difference between the two active current components are fed into the second PI controller to generate the d-axis voltage reference v_d^{ref}. Similarly, the reactive power and AC-side voltage controls are activated by switches 3 and 4, respectively. The output of this switch is then fed into the PI controller to generate reactive current reference i_q^{ref}. The reactive current reference is then sent to the reactive current controller to generate the q-axis voltage reference v_q^{ref}. The generated voltage references v_{dq}^{ref} are then converted into abc form v_{abc} and next into the v_{uabc} and v_{labc} for the upper and lower arm of the MMC converters. The PI control parameters of the outer voltage control loop and the current controllers are given in Table 5.

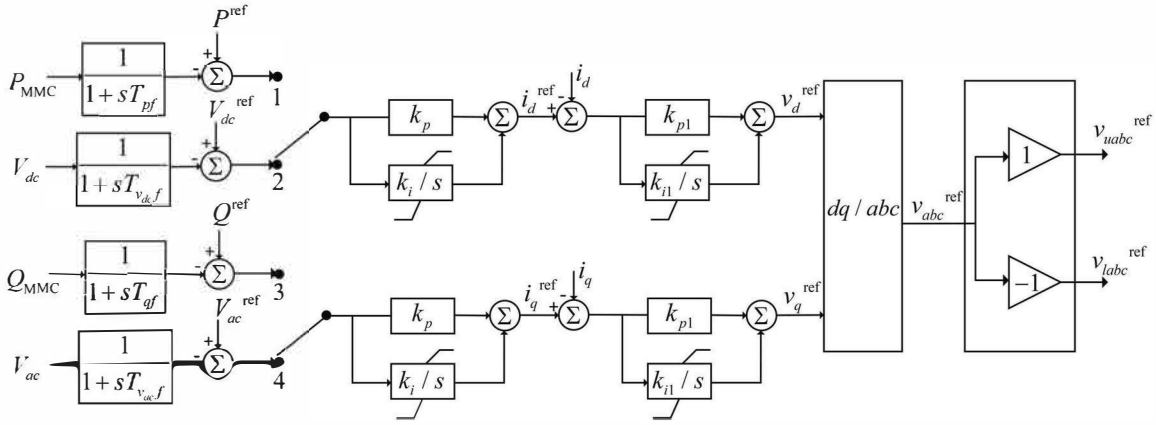

Figure 8. Block diagram of the outer loop voltage control in MMC HVDC converter.

Table 5. Parameters for the outer loop voltage control in MMC HVDC converter

Symbol	Description	Value
K_p	Outer loop proportional control gain	2
K_i	Outer loop integral control gain	1
K_{p1}	Current loop control proportional gain	0.1
K_{i1}	current loop control integral gain	1

3.2 Wind Plant Model and Control

In this work, we leverage the existing Type-4 Wind Turbine Generation (WTG) model in the HYPERsim's example library. The configuration of this model is shown in Fig. 9. This model consists of a wind turbine, a permanent magnetic (PM) machine, a machine-side converter (MSC), dc link, a grid-side converter (GSC), ac filter, and controller systems for both converters.

As the typical control of a WTG model in the literature, the MSC controller performs the MPPT operation and controls the reactive power injection or the voltage at the terminal of the machine. On the other hand, the GSC controller is used to regulate the dc-link voltage at a desired value and control the reactive power injection or the voltage at the GSC terminal. The control blocks representing these operating modes of MSC and GSC are shown in Fig. 10.

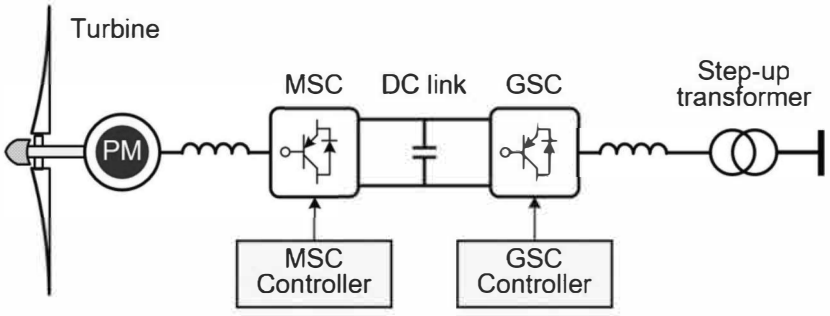

Figure 9. Configuration of a typical type-4 WTG.

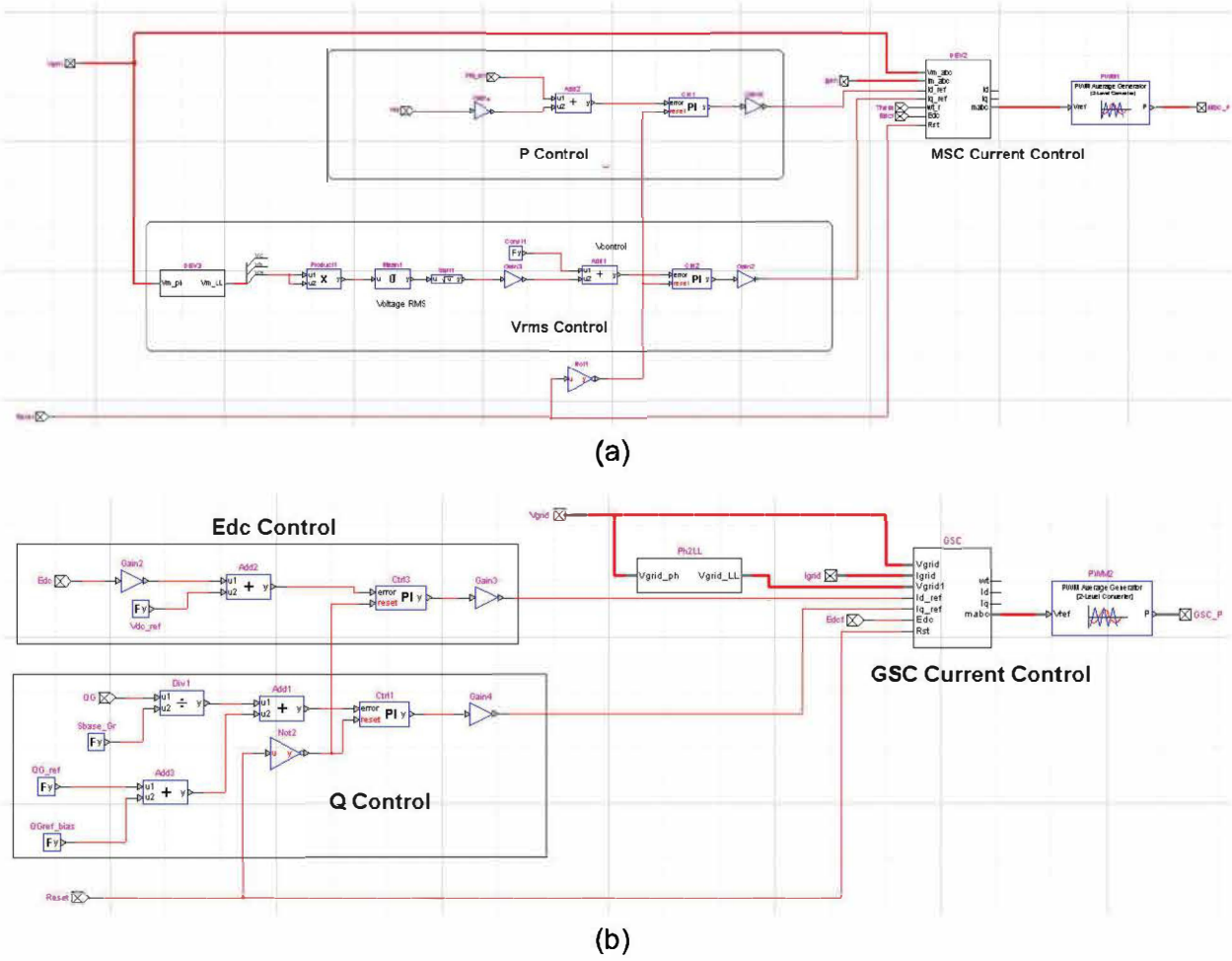

Figure 10. Implementation of a) MSC control and b) GSC control in HYPERsim.

At the MSC, the reference power for the MSC control is determined based on the available wind speed and arero-dynamic model of the WT, in which the implementation in HYPERsim is shown in Fig. 11. Details of WT dynamics, which are widely understood and can be found in [15–17], include:

- Mechanical speed control: The reference mechanical speed of the WTG is calculated based on a GE-based quadratic function of the measured mechanical power or the sum of the measured electrical power and losses [17]. This reference speed is compared with the measured speed to genrate the reference mechanical power for the MSC control shown in Fig. 10(a).

- Pitch control: The pitch control block changes blade pitch angle at higher than rated wind speeds to spill excess power. Thus, power output is maintained at rated value even though wind speed exceeds rated wind speed. In other words, the pitch angle signal is active only when wind speed is higher than the rated speed; otherwise, is fixed at zero.

- Calculation of mechanical torque: The mechanical torque, which is an input of the machine model, is computed based on the Tip-Speed ratio λ, the above calculated pitch angle, air density ρ, rotor radius, and wind speed.

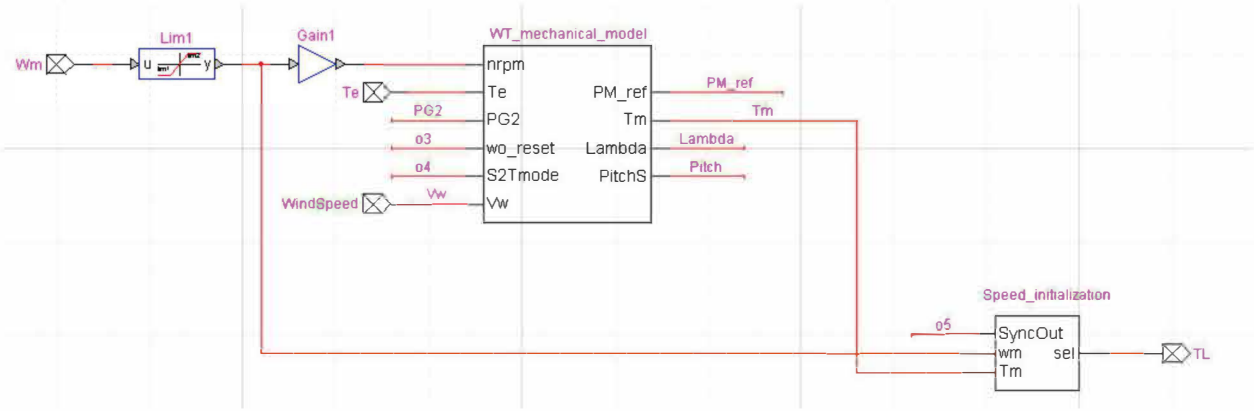

Figure 11. Control block implementing WT dynamics in HYPERsim

3.3 Onshore AC system

Fig. 12 shows the IEEE 9-bus system that represents the onshore HVac grid in Fig. 3. Key system parameters are shown in Table. 6.

Bus 2 of the IEEE 9-bus system is connected to a 18kV/320kV step-transformer before connecting to MMC1 converter of the 2-terminal HVdc system.

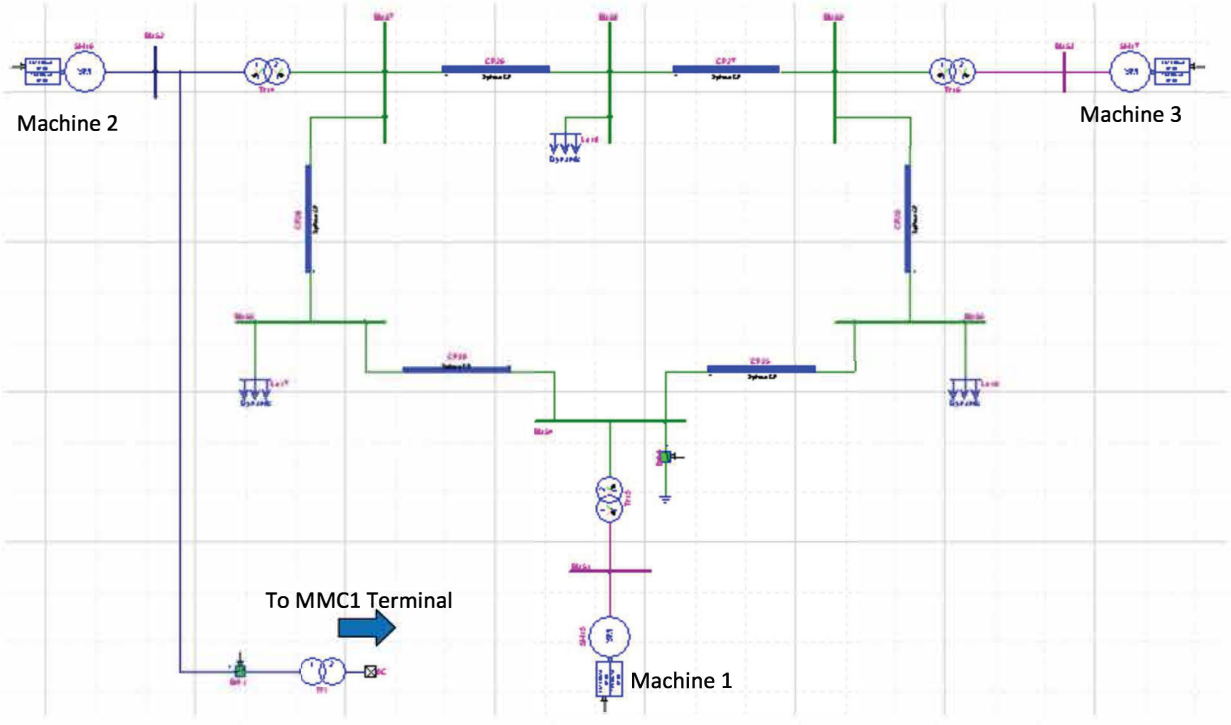

Figure 12. IEEE 9-bus system in HYPERsim with 3 synchronous machines and point of connection to MMC1 terminal.

Table 6. Key parameters of the IEEE 9-bus transmission system.

Parameters	Values
Number of buses and branches/transformers	9 and 9
Number of generators and loads	3 and 3
Primary and secondary voltages	18 kV and 230 kV
Total load	315 MW

4.0 Simulation Results and Discussion

This section presents simulation results and respective discussions on the system responses and HVdc capabilities using the system in Fig. 3 under different operating conditions. Fig. 13 shows the control modes of MMC1 and MMC2 converters, which are set via the high-level control control blocks as shown in Fig. 7. In this studied system, MMC1 is selected to control the real and reactive power injections to the onshore IEEE 9-bus system. On the other hand, MMC2 is selected to control dc voltage and the reactive power injection to the offshore ac island.

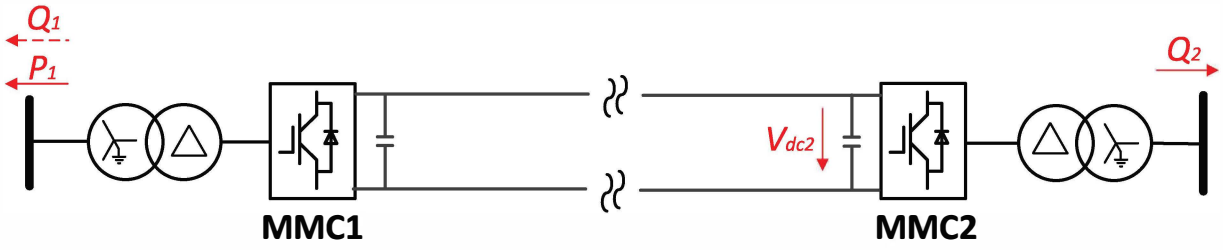

Figure 13. Control modes of MMC1 and MMC2 in the 2-terminal HVdc system

4.1 Detailed Submodule and Arm Voltages

As described in Section 2.0, the high-fidelity MMC model in this work explicitly models each individual SM in an arm, which are shown in Fig. 14. It can be seen that the SMs' capacitor voltages have the saw-tooth waveform due to the charging and discharging process determined by the SM switching modulation.

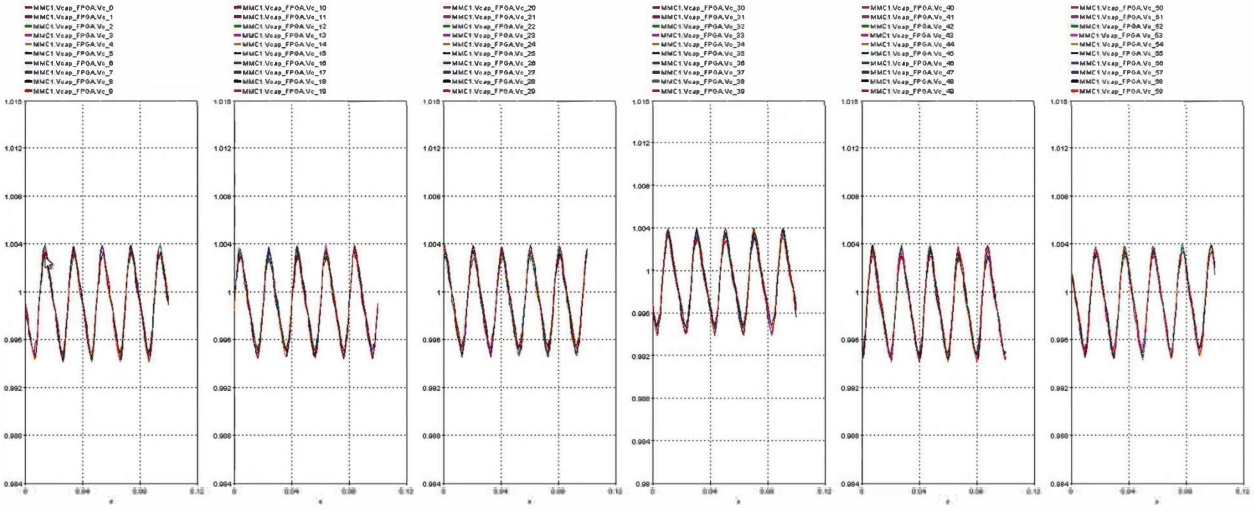

Figure 14. Capacitor voltages of 10 selected SMs pf 6 arms of MMC1 converter.

The reference voltages corresponding to 6 arms of MMC1 converter is shown in Fig. 15, compared to 3-signal reference voltages as in the modulation of 2-level voltage source converters.

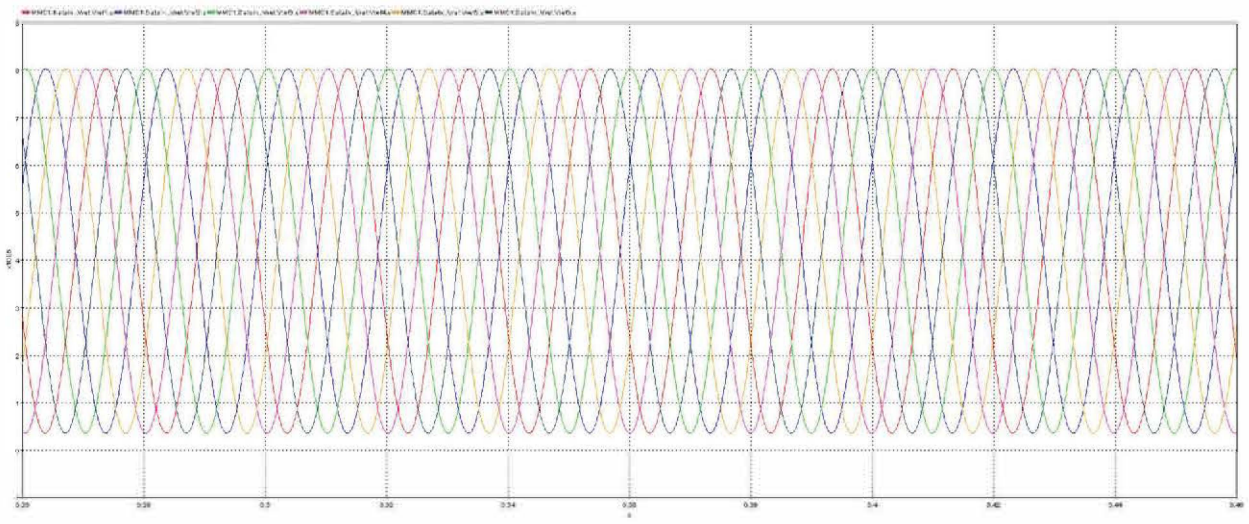

Figure 15. 6-signal reference voltages for 6 arms of MMC1 converter.

4.2 Power Rescheduling at the Onshore Terminal

Due to different operating conditions of the onshore HVac grid, it is necessary for an HVdc transmission system to be able to reschedule real and reactive power to provide frequency and voltage supports.

4.2.1 Real Power Rescheduling

To demonstrate the real power rescheduling capability of the 2-terminal HVdc system in Fig. 3, a step change of the real power setpoint of Terminal 1 from 0.1 pu to 0.2 pu is applied at 2 second. It can be seen from Fig. 16 that the actual power injection at Terminal 1 closely follows the step change of the setpoint. The real power injection to the HVdc system from the offshore wind side, which cannot be controlled directly, is approximately equal to the real power at Terminal 1. A small difference between the two real power injections at the two terminal is due to converter and dc-line losses.

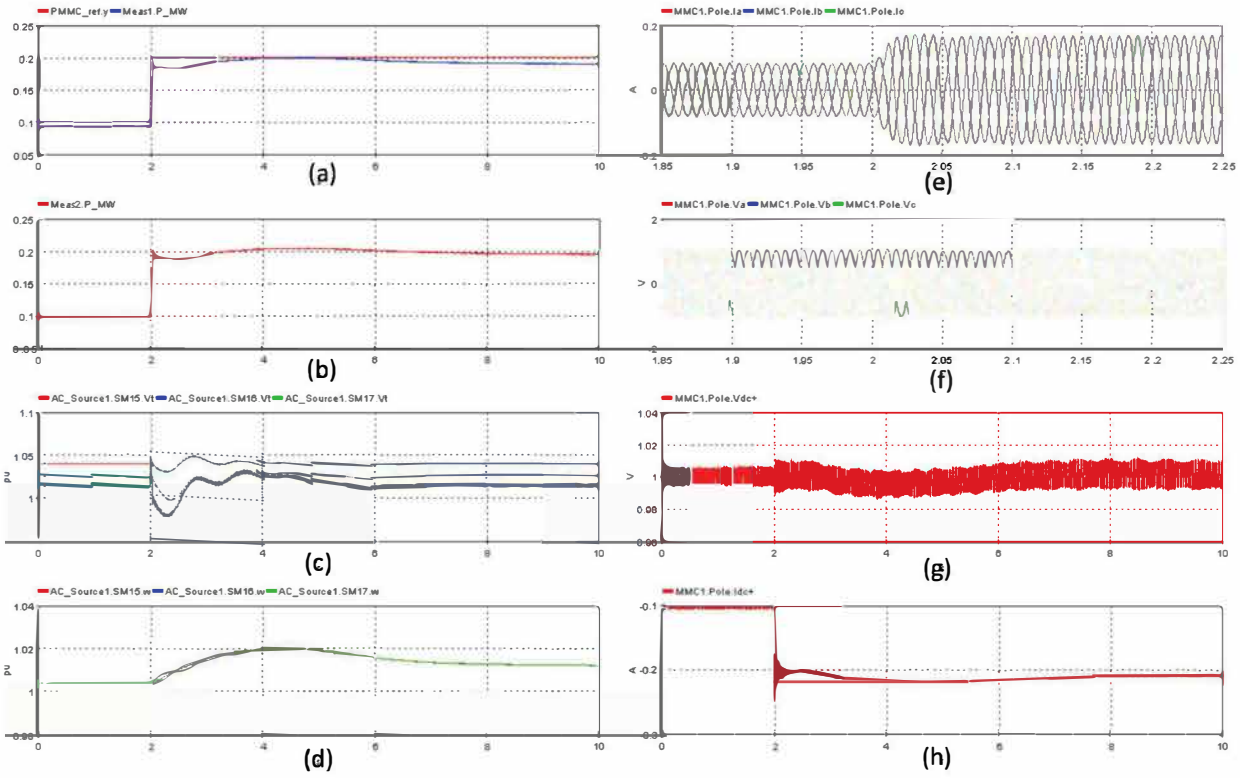

Figure 16. Real power rescheduling: a) The reference and actual real power injection at the ac side of MMC1, b) actual real power injection to MMC2 from the offshore wind, c) and d) voltage magnitudes and frequencies at 3 machines in the IEEE 9-bus system, e) and f) instantaneous voltage and current at the ac side of MMC1, g) and h) dc voltage and current at the dc side of MMC1

4.2.2 Reactive Power Rescheduling

Unlike the real power control, each terminal can control the reactive power separately from each other. A step change of reactive power at Terminal 1 from 0.2 pu to 0.1 pu is applied at 2 second. It can be seen from the simulation result in Fig. 17 that the actual reactive power injection at the ac side of MMC1 closely follows the reference value. On the other hand, the reactive power at the ac side of MMC2 converter does not get affected. In the IEEE 9-bus system, although there is an increasing in reactive power injection at Bus 2 from MMC1 converter, the voltage magnitude at this bus does not significantly increase because of the local voltage controller of the Machine 2 at this bus. On the other hand, the current magnitude reduces because of the reactive power reduction,

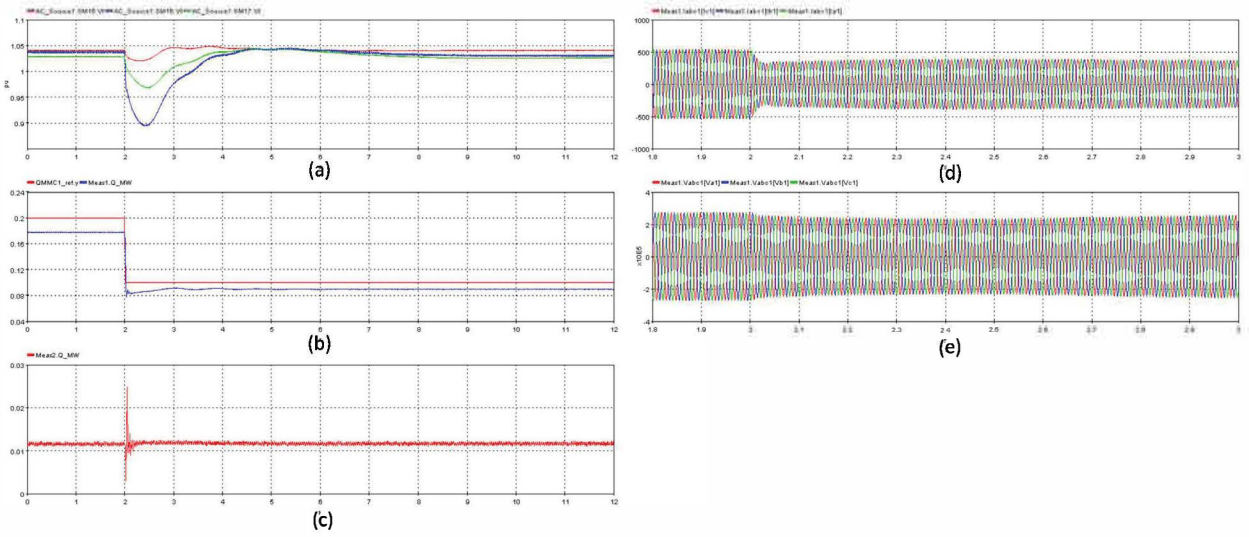

Figure 17. Reactive power rescheduling: a) The reference and actual real power injection at the ac side of MMC1, b) actual real power injection to MMC2 from the offshore wind, c) and d) voltage magnitudes and frequencies at 3 machines in the IEEE 9-bus system, e) and f) instantaneous voltage and current at the ac side of MMC1, g) and h) dc voltage and current at the dc side of MMC1

4.3 DC Faults

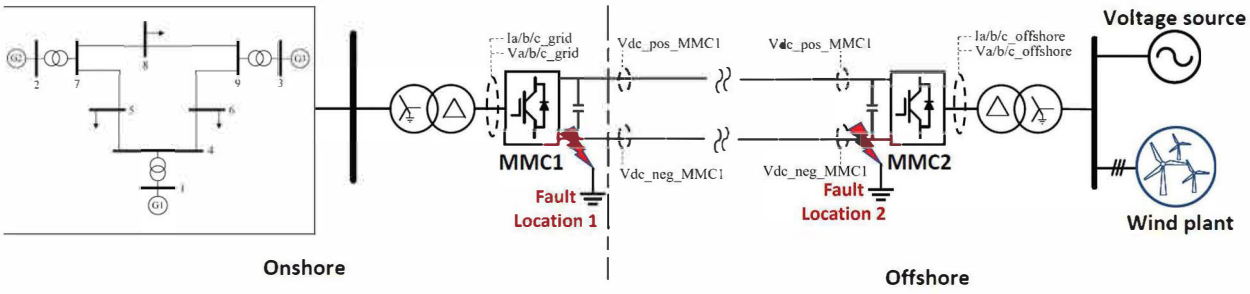

Figure 18. Injection of Line to Ground (LG) faults on the DC lines at two locations

One of the main interests for an HVdc or an MTdc system is system response under dc faults. This section discusses about the simulation results for various faults injected in the 2-terminal HVdc system. Specifically, pole to pole to ground faults (similar to 3-phase to ground faults in AC systems) were injected at two locations (as shown in Fig. 18) and for two different periods of time, leading to four scenarios as shown in Table 7.

The plots in Figs. 19, 20, 21, and 22 measure the system dynamics for both MMC1 and MMC2, including the DC and AC sides of the converters, and the IEEE 9-bus system synchronous machine dynamics. In scenario 1 (Fig. 19), the fault location is on the DC side of MMC1, which connects the onshore IEEE 9-bus system (grid side) to the HVdc line as shown in Fig. 18 and the fault duration is $20\ ms$. The impacts of the faults on the grid side are evidently seen in the 3-phase current and voltage plots starting at $t = 25\ s$. The oscillations die down within a few

Table 7. Scenarios tested for DC fault evaluation

Scenario	Fault Location (DC)	Fault Start Time (simulation time)	Fault Duration
1	$MMC1$	$25\ s$	$20\ ms$
2	$MMC1$	$25\ s$	$50\ ms$
3	$MMC2$	$45\ s$	$20\ ms$
4	$MMC2$	$45\ s$	$50\ ms$

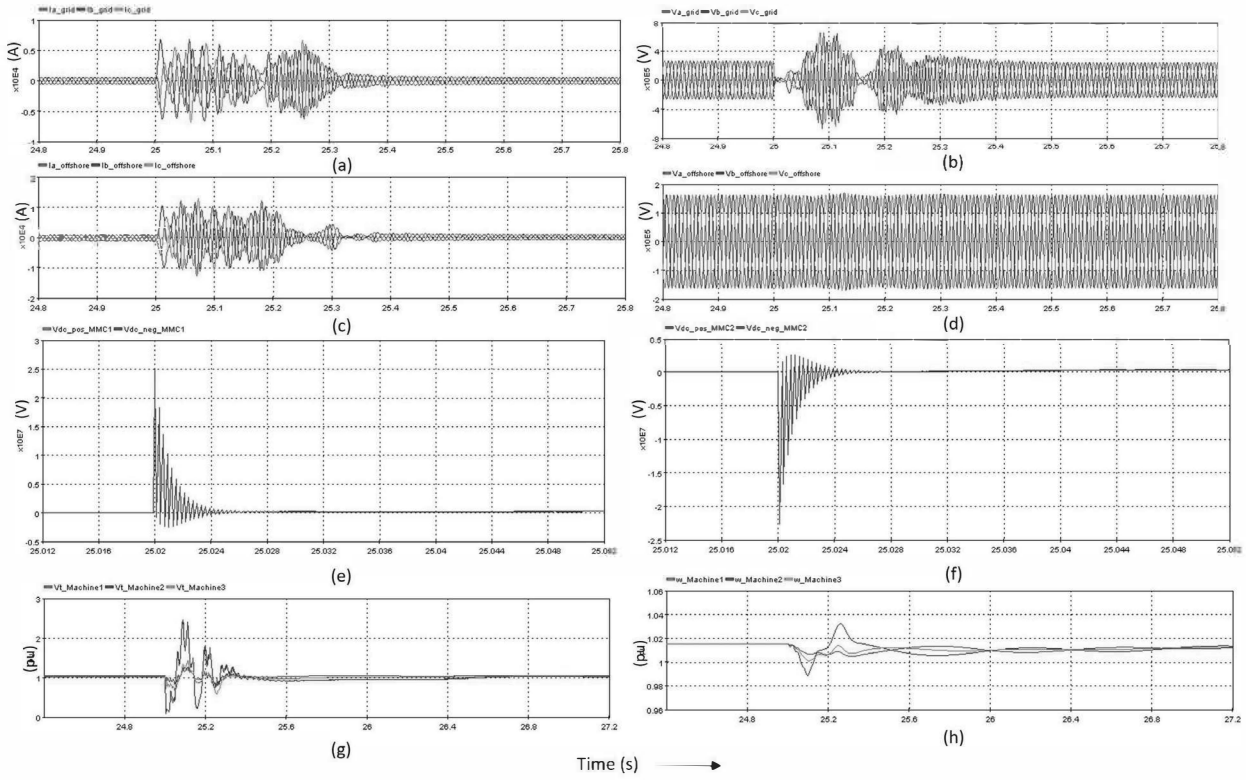

Figure 19. System response for scenario 1: (a) Grid Currents (b) Grid Voltages (c) Offshore System Currents (d) Offshore System Voltages (e) & (f) DC voltages for MMC1 and MMC2, respectively, (g) Terminal voltages of synchronous machines (h) Frequency response of the machines

hundred milliseconds both on the grid and the offshore side. The oscillations in the currents on the offshore side are more pronounced than in the voltage waveforms due to the fact that there is a strong voltage source connected to the offshore wind plant to make the system more stable. In future studies, grid-forming control of MMC2 will eliminate the need for this voltage source. The effects of the dc side fault are also seen in the synchronous machine outputs. The transients in the terminal voltage and the frequency of the generators are of higher magnitudes in Machine 2 as it is directly connected to MMC1 through a transformer.

Fault injection in scenario 2 is at the same location as scenario 1, but the duration of the fault is higher ($50\ ms$). The oscillations in the system sustain for a much longer period of time, of up

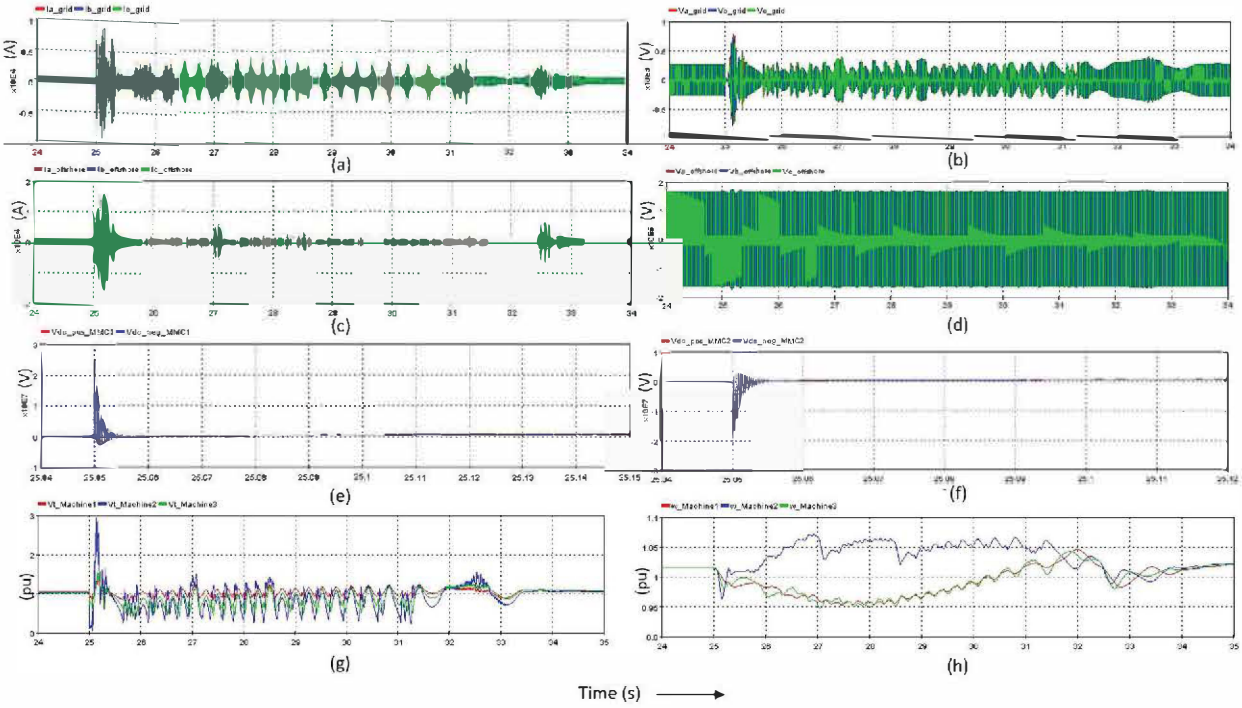

Figure 20. System response for scenario 2 (refer to Fig. 19 for the subplot description)

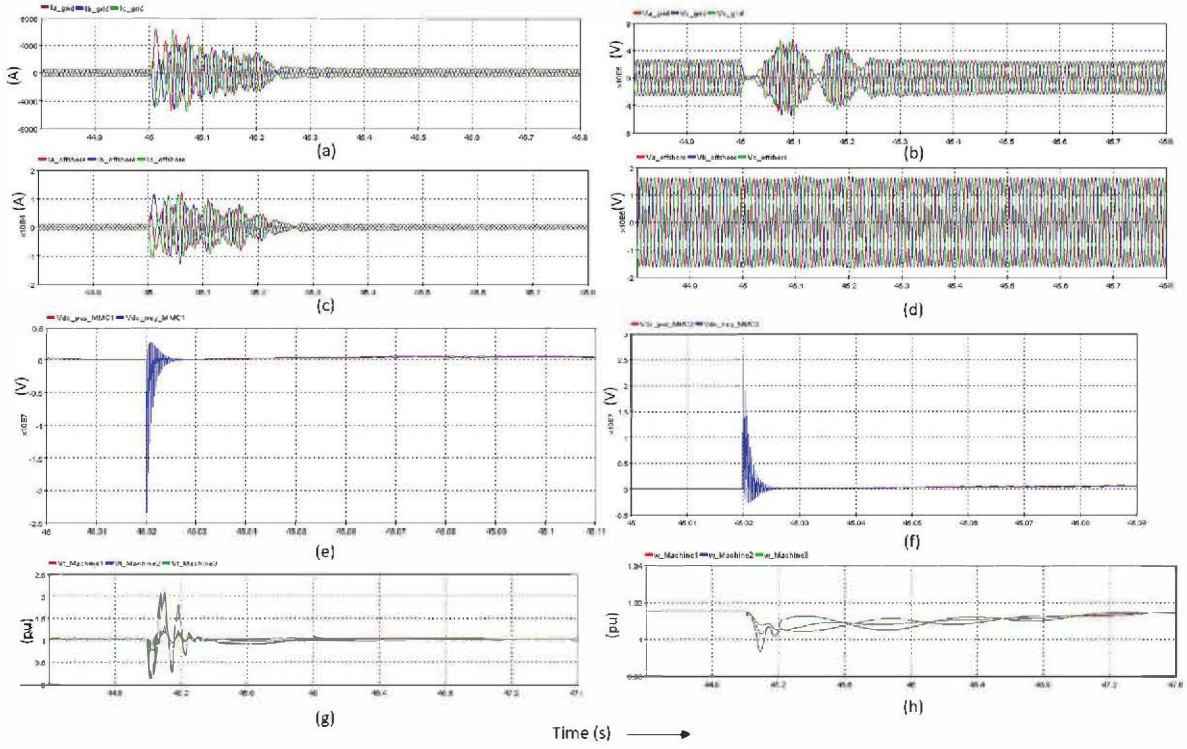

Figure 21. System response for scenario 3 (refer to Fig. 19 for the subplot description)

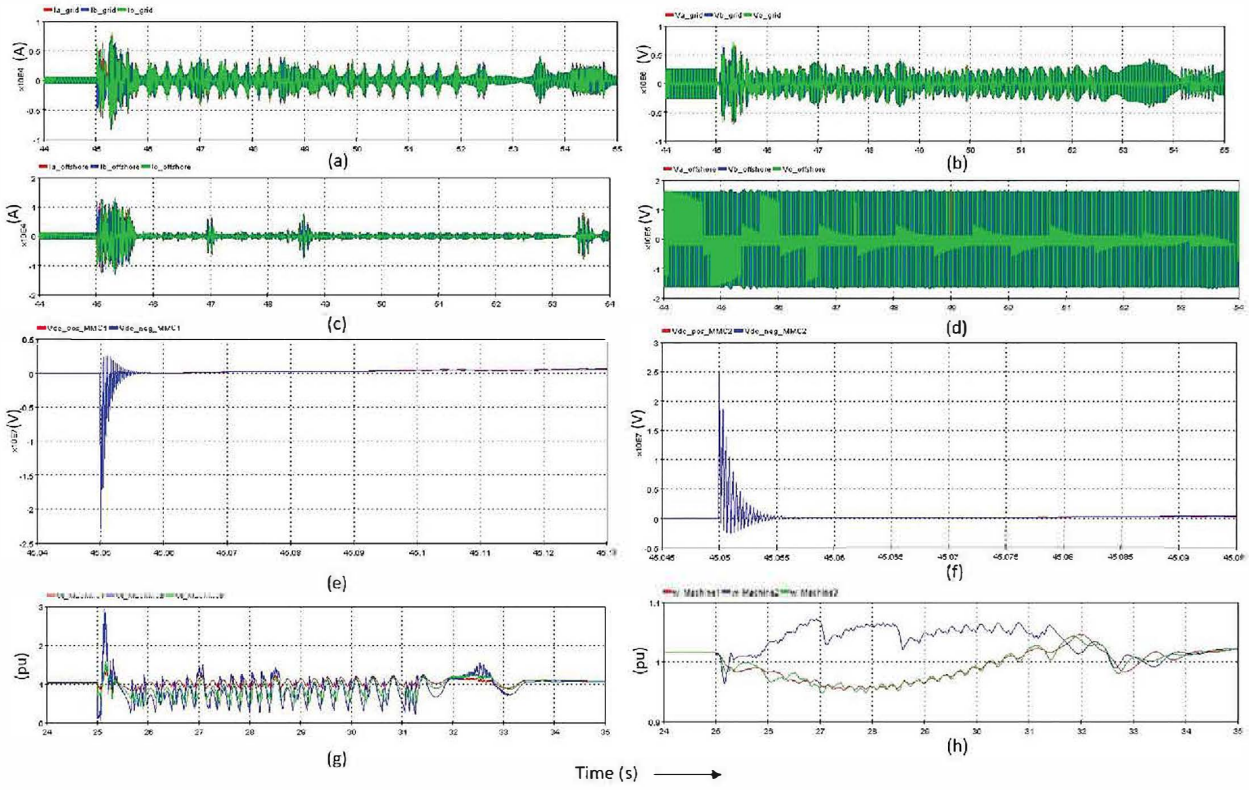

Figure 22. System response for scenario 4 (refer to Fig. 19 for the subplot description)

to 10 seconds, which would have triggered the protection schemes, if implemented, and tripped the lines. It is interesting to note that even though the DC system oscillations die down within a few hundred milliseconds, the AC system takes another close to ten thousand milliseconds to stabilize. In scenarios 3 & 4, the fault is injected on the DC side of MMC2 for $20\ ms$ and $50\ ms$ fault duration, respectively. In these scenarios, even though the transients are slightly smaller in magnitude on an average, compared to the faults near MMC1, the response is very similar in both the cases, showing that the location of the fault on the dc line has insignificant contribution in the impact of the faults when compared to the fault duration.

4.4 AC Faults

In addition to dc faults, ac faults are also studied to understand the impact and propagation of such ac-side disturbances to the dc side. Two fault scenarios are introduced. In the first scenario, a bolted fault occurs at a load bus far from MMC1 terminal at 2 second and lasts for 0.2 second. In the second event, aa similar fault occurs at MMC1 terminal.

The simulation results of the two fault scenarios are shonw in Figs. 24 and 25.

- The entire system is able to ride through these ac faults after initial transient periods. All controlled quantities return to the pre-event setpoints.
- Since no voltage and frequency supports are implemented for the 2-terminal HVdc system, the MMC1 converter at Terminal 1 does not provide any contributions to support the IEEE 9-bus system.

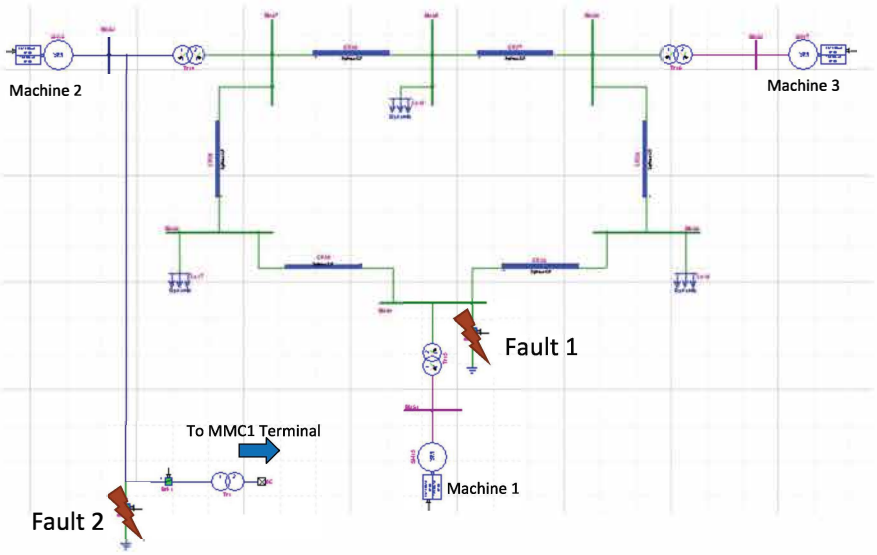

Figure 23. Locations of 2 ac faults in the IEEE 9-bus systems

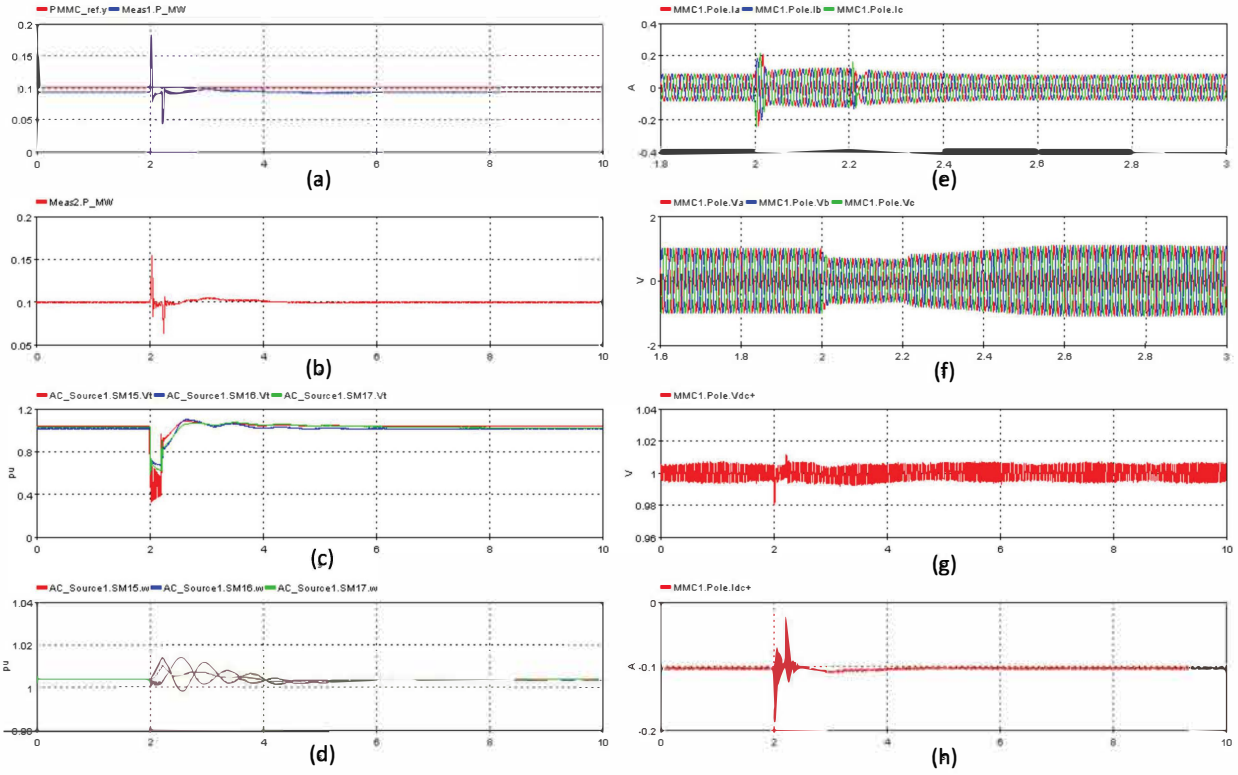

Figure 24. ac-fault 1 scenario (fault location far from MMC1 terminal): a) The reference and actual real power injection at the ac side of MMC1, b) actual real power injection to MMC2 from the offshore wind, c) and d) voltage magnitudes and frequencies at 3 machines in the IEEE 9-bus system, e) and f) instantaneous voltage and current at the ac side of MMC1, g) and h) dc voltage and current at the dc side of MMC1

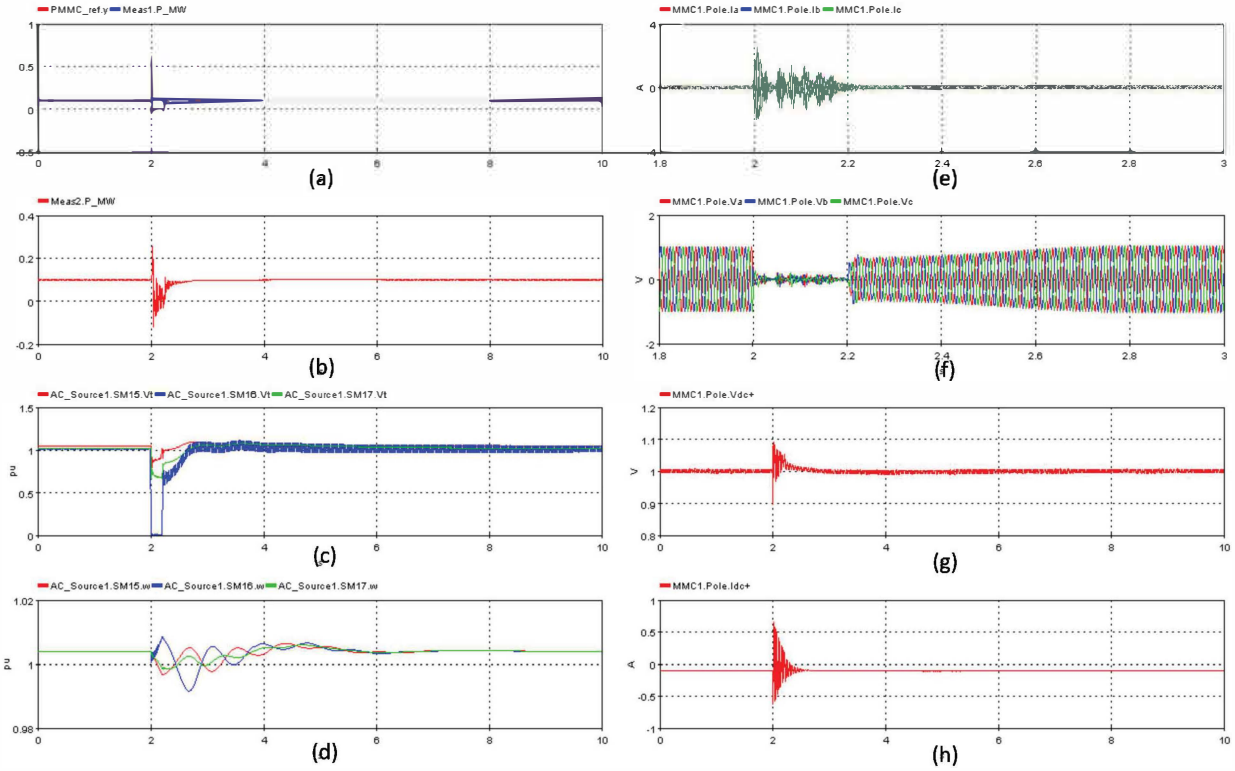

Figure 25. ac-fault 2 scenario (fault location at MMC1 terminal): a) The reference and actual real power injection at the ac side of MMC1, b) actual real power injection to MMC2 from the offshore wind, c) and d) voltage magnitudes and frequencies at 3 machines in the IEEE 9-bus system, e) and f) instantaneous voltage and current at the ac side of MMC1, g) and h) dc voltage and current at the dc side of MMC1

- Within the HVac grid, the electrical distance between the fault location and 2 machines results in expected levels of machine voltage sags. A shorter the electrical distance leads to a deeper terminal voltage sag.
- Since the fault at the second scenario is closer to MMC1 terminal, it affects the dc voltage and current during the transient more, compared to those in the first scenario when the fault is far from MMC1 terminal.

4.5 Wind Speed Variations

To verify the efficacy of the wind plant model connected to Terminal 2 of the HVdc system, this section shows the response of the wind plant under different wind speeds. Initially, the wind speed is at the rated speed of 11.3 m/s. At 20 second, the wind speed decreases to a step change of wind speed from the rated speed of 10.17 m/s. At 80 second, the wind speed increase to 12.43 m/s, exceeding the rated speed.

Fig. 26 shows the responses of the WTG model under the above varying wind condition. It can be seen from the simulation results that:

- The wind plant remains stable after initial transients caused by the wind speed variations.
- The actual machine speed closely follows the reference speed.
- The pitch angle only takes effect when the wind speed exceeds the rated speed at 80 second.
- Regarding WTG control, the mechanical power and machine voltage closely follow the referenced values. Similarly, the reactive power and dc-link voltage in the GSC control also accurately track the reference values. These results show the efficacy of the MSC and GSC control in the WTG model.

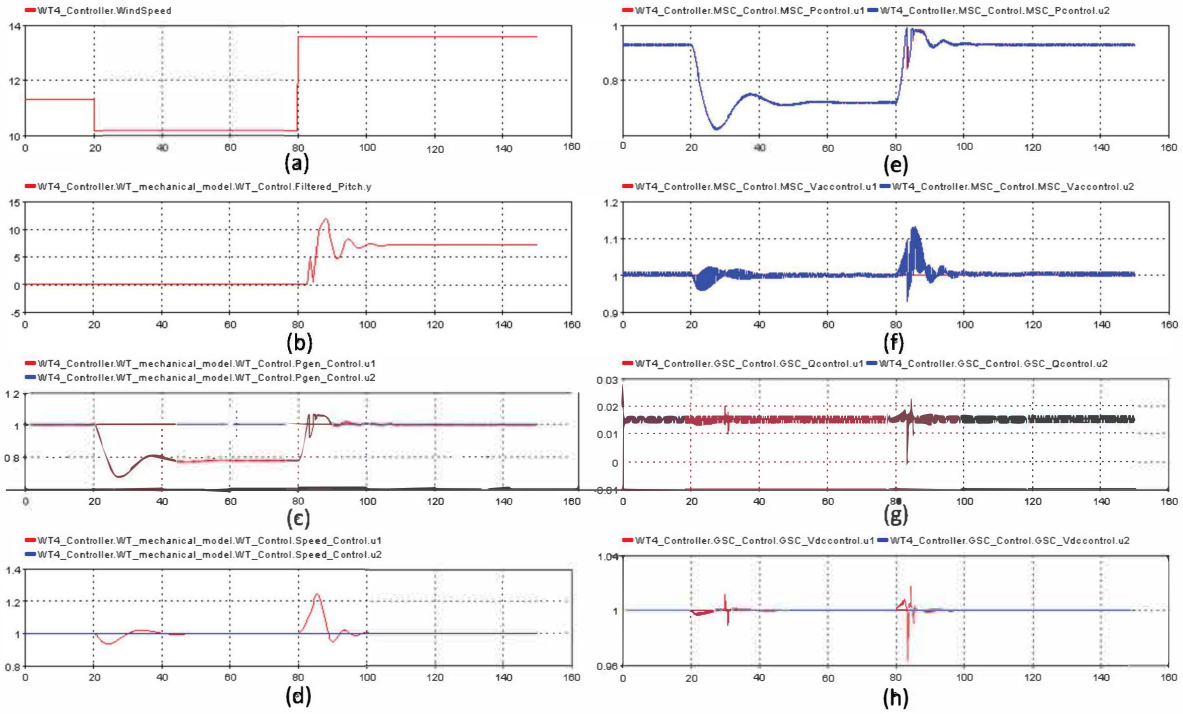

Figure 26. ac-fault 2 scenario (fault location at MMC1 terminal): a) Wind speed, b) pitch angle, which is the output of the pitch control, c) rated and actual electrical power, d) reference and actual machine speed, e) reference and actual mechanical power in the MSC control, f) reference and actual terminal voltage of the PM synchronous machine in the MSC control, g) reference and actual reactive power in the GSC control, h) reference and actual dc-link voltage in the GSC control.

5.0 Technical Challenges when Extending to Multi-Terminal HVdc Systems

5.1 CPU and FPGA interaction schemes

Complex topologies such as MMCs are challenging to analyze and simulate in high-fidelity environments using purely CPU based simulation approaches. While utilizing FPGA based approaches makes it possible to simulate MMCs with a high level of accuracy and fidelity, a setup using FPGA+CPU based simulation techniques is limited in some ways. Since, execution on FPGAs involves designing a set of lower level commands on logic arrays, the model developed is relatively inflexible after it has been designed. For instance, while certain parameters such as passive impedances, the number of submodules in each arm or the carrier frequency can be modified, larger modifications are not possible. This is because the FPGA based models are a series of logic steps that are programmed and designed with specific execution delays to enable accurate simulation while interacting with system level models on the CPU. Thus, the limitation in terms of modifications arises from the bitstream generated to allow CPU interaction with the FPGA as well as the model instruction set to replicate an MMC on the FPGA. This means that any sizable change to the MMC model or the nature of the CPU's interaction with the model would involve identifying and designing CPU and FPGA interaction schemes (bitstreams) as well as redesigning, synthesizing, verifying and integrating a new instruction set representing an MMC with new exchange parameters and topology on the FPGA. The solution explored in this report is a 2-terminal MMC. For instance, exploring a 4-terminal MMC would entail a new bitstream and FPGA instruction set.

5.2 High Computational Capability Requirement

The second main limitation is the compute capability. OPAL-RT simulators are armed with an FPGA board with an array of CPUs to conduct power system simulation. The number of logic arrays currently on a standard simulator are capable of simulating 2 terminal MMC systems. While this is significant, expanding to a 4 terminal system would require significantly more gated array capabilities. To do this an expansion setup would have to built where an additional FPGA can be linked to the preexisting one through an optical cable to ensure rapid exchange of data. Thus an OPAL-RT simulator with CPUs and FPGAs linked to an FPGA expansion kit would be sufficient to meet the compute capabilities required to reach this goal. An adequate bitstream and instruction set can be explored with the vendor to allow this solution to be realized.

5.3 MMC Converter Control Design and Implementation

The MMC controller presented in this study is developed based on the grid-following approaches which takes some predefined references and generates control actions to track them. However, with the recent increased interest of grid-forming technologies in the modern power system, the MMC converter controllers presented in this study can be improved with the grid-forming approaches. Having an MMC-based strong grid-forming source can enable integration of power electronic devices and eliminate the requirements of strong AC sources on the offshore wind side. Therefore, future studies for multi-terminal HVdc system can leverage the developed 2-terminal grid-following MMC-based HVdc model in this project to explore the following topics:

- $V_{dc} - P_{dc}$, $P_{ac} - f$, and $Q_{ac} - V_{ac}$ based droop control strategies will be explored to test the grid-forming capabilities of the MMC converters in a multi-terminal HVdc system. As shown in the previous sections, it is likely that the high-level control implemented in HYPERsim needs to be modified. In addition, with the change in control strategy, the list and configuration for data exchange between CPU and FPGA also need to be re-programmed.

- Co-optimize research might lead to new substation configuration design. As explained in Section 5.1, it requires modifications and validations in the number of exchanged data and bitstream reconfiguration.

- Some secondary control with objectives of optimal power sharing, power loss mitigation, and advanced reinforcement learning (RL) based protection strategies will be also incorporated in the future study. These goals also require significant changes in design and implementation.

6.0 Conclusion

This section summarizes the most important results and achievements from the proposed work.

- In Section 2.0, a brief literature review about MMC converter, high-level and low-level converter control, and modeling capability of MMC converters in OPLA-RT is conducted. Given the complexity of MMC modeling and control, OPAL-RT offers a high-fidelity modeling approach for MMC converters in a real-time simulation platform.
- Section 3.0 presents a detailed discussion on the modeling and implementation of MMC converters and WTG in OPAL-RT. The knowledge obtained from this sections greatly improve understanding about OPAL-RT modeling capability for MMC converters.
- Section 4.0 shows the simulation results of a 2-terminal HVdc transmission that deliver offshore wind to an onshore HVac test system under various operating conditions. These simulation results validate the modeling and control described in Section 3.0.
- Section 5.0 provides a list of technical challenges when extending the developed 2-terminal HVdc transmission system to a multi-terminal HVdc transmission system in OPAL-RT, including potential changes in modeling and control strategies. These knowledge is greatly beneficial for future projects related to multi-terminal HVdc transmission systems.

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