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L•PRIZE®

Stress Testing of the Philips 60W Replacement Lamp Entry

April 2012

Prepared for:

Solid-State Lighting Program
Building Technologies Program
Office of Energy Efficiency and Renewable Energy
U.S. Department of Energy

Prepared by:

Pacific Northwest National Laboratory

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Stress Testing of the Philips 60W Replacement Lamp L Prize Entry

U.S. Department of Energy
Solid-State Lighting L Prize Competition

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Executive Summary

The Pacific Northwest National Laboratory, operated by Battelle for the U.S. Department of Energy, worked with Intertek to develop a procedure for stress testing medium screw-base light sources. This procedure, composed of alternating stress cycles and performance evaluation, was used to qualitatively compare and contrast the durability and reliability of the Philips 60W replacement lamp L Prize entry with market-proven compact fluorescent lamps (CFLs) with comparable light output and functionality. The stress cycles applied simultaneous combinations of electrical, thermal, vibration, and humidity stresses of increasing magnitude. Performance evaluations measured relative illuminance, x-chromaticity and y-chromaticity shifts after each stress cycle.

The Philips L Prize entry lamps appear to be appreciably more durable than the incumbent energy-efficient technology, as represented by the evaluated CFLs, and with respect to the applied stresses. Through the course of testing, all 15 CFL samples permanently ceased to function as a result of the applied stresses, while only 1 Philips L Prize entry lamp exhibited a failure, the nature of which was minor, non-destructive, and a consequence of a known (and resolved) subcontractor issue.

Given that current CFL technology appears to be moderately mature and no Philips L Prize entry failures could be produced within the stress envelope causing 100 percent failure of the benchmark CFLs, it seems that, in this particular implementation, light-emitting diode (LED) technology would be much more durable in the field than current CFL technology. However, the Philips L Prize entry lamps used for testing were carefully designed and built for the competition, while the benchmark CFLs were mass produced for retail sale—a distinction that should be taken into consideration. Further reliability testing on final production samples would be necessary to judge the extent to which the results of this analysis apply to production versions of the Philips L Prize entry.

Acronyms and Abbreviations

AC	alternating current
CFL	compact fluorescent lamp
DOE	U.S. Department of Energy
EISA	Energy Independence and Security Act of 2007
FMVT	Failure Mode Verification Testing
HALT	Highly Accelerated Life Testing
LED	light-emitting diode
PNNL	Pacific Northwest National Laboratory
SSL	solid-state lighting

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1.0 Introduction

The Energy Independence and Security Act of 2007 (EISA) directed the U.S. Department of Energy (DOE) to establish the Bright Tomorrow Lighting Prize (L Prize) competition. The L Prize (DOE 2011a) is the first government-sponsored technology competition designed to spur lighting manufacturers to develop high-quality, high-efficiency solid-state lighting (SSL) products to replace the common light bulb. The L Prize competition is one of a number of ongoing efforts that form the foundation of the DOE SSL Program (Figure 1.1), which is aimed at accelerating and guiding technology advances from the laboratory to the marketplace (DOE 2011b).

Figure 1.1. DOE SSL Program Approach

The L Prize guidelines include technical specifications to ensure compliance with the general requirements outlined in EISA and additional specifications for quality, performance, and mass manufacturing. The competition also includes a comprehensive evaluation process for proposed products, designed to detect and address product weaknesses before market introduction, to avoid problems with long-term market acceptance. The comprehensive product evaluation includes performance, lifetime, and stress testing conducted by DOE national and independent laboratories, and field assessments conducted in collaboration with utilities and other partners.

In September 2009, the L Prize competition received its first entry, a 60-watt (60W) replacement lamp product from Philips Lighting North America (Philips). In Spring 2010, the Philips 60W replacement lamp entry completed photometric testing, the first stage of the evaluation process. In June 2010, field assessments and long-term lumen maintenance testing began. With photometric and lumen maintenance testing results looking promising and field assessments completed, planning for stress testing began in early 2011. This report describes stress test design and implementation, summarizes testing results, and offers analysis and conclusions derived from those results.

2.0 Stress Test Development

Pacific Northwest National Laboratory (PNNL) accepted project management responsibility for L Prize evaluation stress testing. PNNL identified and contacted Intertek for assistance with the stress test design and execution based on their extensive experience in this field. In preliminary discussions, Intertek's patented Failure Mode Verification Testing (FMVT®) process (Intertek 2011), given its ability to produce multiple failure modes in a relatively short amount of time, was recognized as having high potential to meet the needs of the L Prize evaluation. Like most highly accelerated stress-testing processes, FMVT consists of applying an increasing level of stress over the course of multiple steps and evaluating functional behavior after each step. FMVT differs from Highly Accelerated Life Testing (HALT) in two key areas (Intertek 2004). First, HALT identifies failures by applying one stress at a time to determine operational and destruct limits of the product from each stress source; FMVT applies stress sources simultaneously, beginning at service conditions and increasing to a predetermined maximum test level. Second, with HALT, the margin between the service conditions and the operational and destruct limits provides the basis for analyzing the relevance of the failure modes; FMVT uses the number of failure modes, the time to failure, and the relative distribution in time of the failures to determine the maturity of the design and the benefits of addressing specific failure modes. The FMVT plan for a specific product or technology evaluation is developed with five specific target goals:

1. Choose stresses that the product or technology will see during actual use
2. Produce multiple failure modes
3. Test to failure
4. Conduct failure analysis
5. Estimate design maturity

Medium screw-based replacement lamps are installed in a wide variety of environments and subject to multiple potential stresses. A brief review of typical installation environments and the capabilities and costs for applying stresses available at the Intertek facility led to the decision to design cycles that apply simultaneous combinations of electrical, thermal, vibration, and humidity stresses. Equipment for applying the chosen stresses was identified, and additional equipment for mounting and functionally verifying the test samples between stress cycles was designed and built.

A preliminary, 10-step FMVT stress plan was created, focusing on testing to failure. The stress levels used in the FMVT stress plan began at applying service, or expected typical use (step 1) and ended at applying expected destruct levels (step 10). Time and cost constraints suggested that the test plan should be designed to be completed in one business week (5 days) or less. Therefore, actual test time (i.e., alternating cycles of stress application and functional verification), was budgeted for around 30 hours, leaving 10 hours for setup and troubleshooting.

Highly accelerated stress testing, in general, and FMVT, in particular, are well-suited for rapidly and cost-effectively evaluating robustness and identifying potential failure modes of a product. If any failure modes can be associated with design flaws, or slowed by design improvements, then such testing has the potential to lead to the development of improved products with potentially higher reliability and/or longer lifetimes. However, testing typically cannot estimate reliability or lifetime for a variety of reasons. Reliability or lifetime estimation requires the ability to correlate accelerated times to failure during testing

to times to failure in the field. Such correlation is routinely done for products with a limited number of known failure modes which have been proven to be the dominant cause of failure during normal operation, and which can be accelerated in a predictable way without introducing other failure modes. In the absence of such knowledge, the quantitative results of such testing must be kept in perspective.

SSL technology is still rapidly evolving, with innovation happening across all associated component technologies (e.g., light-emitting diode [LED] chips; packaging and integration with phosphors, heat sinks, and optics; design into functional lamps and luminaires). Furthermore, L Prize entries, by definition, are not mature, mass-produced products, free of limiting design flaws and with known failure modes. Thus, FMVT could not be used to estimate the reliability or lifetime of a given entry. However, the medium screw-based replacement lamp market has a long history and is dominated by mature products, which allows FMVT to evaluate more than simply overall product robustness. By simultaneously testing the L Prize entry alongside one or more mature equivalent products with proven reliability and lifetime, the performance of the L Prize entry can be qualitatively evaluated with respect to the benchmark product(s). In order to make this approach as viable as possible, the mature medium screw-based replacement lamps needed to be comparable to the L Prize lamp (i.e., roughly equivalent lighting performance, functionality, and energy efficiency). Consequently, compact fluorescent benchmark lamps were chosen over less-efficient incandescent or halogen lamps.

Functional verification is required following the completion of each stress step to determine if the stress has degraded the performance of any of the samples under evaluation. Functional verification of light sources can be evaluated to varying depths. Most simply, if the source is no longer emitting light at the completion of the stress step, it has certainly failed. Ideally, more qualitative lighting performance measurements would be verified to determining if the sample is still operating as specified. A minimal set of evaluated metrics might include those reported on the DOE LED Lighting Facts (DOE 2011c) label (i.e., light output [or luminous flux], power, efficacy, color rendering index, and correlated color temperature). However, evaluating those metrics using standardized methods (e.g., IES LM-79 testing using an integrating sphere) is unfortunately time-consuming and costly.

Instead, a comparative approach was pursued to balance the desire for measurement relevance with time-expediency and cost. New samples of both the L Prize entry and the benchmarks lamps were evaluated using appropriate standardized methods prior to stress testing to establish baseline sample performance. Then, a custom apparatus, capable of rapidly measuring light output and chromaticity, was designed and built. Initial measurements using the custom apparatus established alternative baselines to use in generating relative measurements following the completion of each stress step. If necessary, the relative degradation in light output or shift in chromaticity measured using the custom apparatus can be applied to the baseline performance data to estimate absolute performance.

The heretofore summarized test setup, test plan, and test sample selection are reviewed in more detail in the following sections.

2.1 Test Setup

The test setup consisted of equipment for applying and controlling stress selected from the equipment pool at the Intertek lab, custom-built equipment specifically designed for rapid mounting and evaluation of medium screw-base replacement lamps, and a light meter for functional verification (Table 2.1).

The test setup for applying and controlling stress was composed of an environmental chamber paired with an FMVT control system. A custom-built stress test board, which provided mechanical and electrical interfaces to 18 medium screw-based lamps (Figure 2.1), was mounted to a vibration table head (Figure 2.2) enclosed in an environmental chamber capable of adjusting air temperature through the use of either heating or cooling elements, and raising the humidity of the enclosed air space (Figure 2.3). The medium screw-base (Edison socket) lampholders were wired in parallel for nominal alternating current (AC) operation, and connected to a digitally controlled AC power supply, programmed to implement the electrical stress plan. The FMVT control system, in concert with sensor inputs and other measurement equipment, implemented and verified the fast-ramp thermal stresses and low-frequency random six-axis uniform vibrational stresses. The test setup was not capable of measuring humidity, and consequently humidity was not under closed-loop control by the system.

Table 2.1. Test Equipment

Description	Model/Asset Number
FMVT control system	130045 (Intertek)
Environmental chamber	130085 (Intertek)
AC power supply	130093 (Intertek)
Digital multimeter	130313 (Intertek)
Oscilloscope	130035 (Intertek)
Accelerometer	130131 (Intertek)
Stress test board	Custom built
Functional verification measurement chamber	Custom built
Functional verification downlight(s)	Lithonia Lighting LP6N-609AZ
Downlight chassis	Custom built
Illuminance/color meter	Konica Minolta CL-20 (PNNL)

Figure 2.1. Stress Test Board, Showing Electrical Wiring

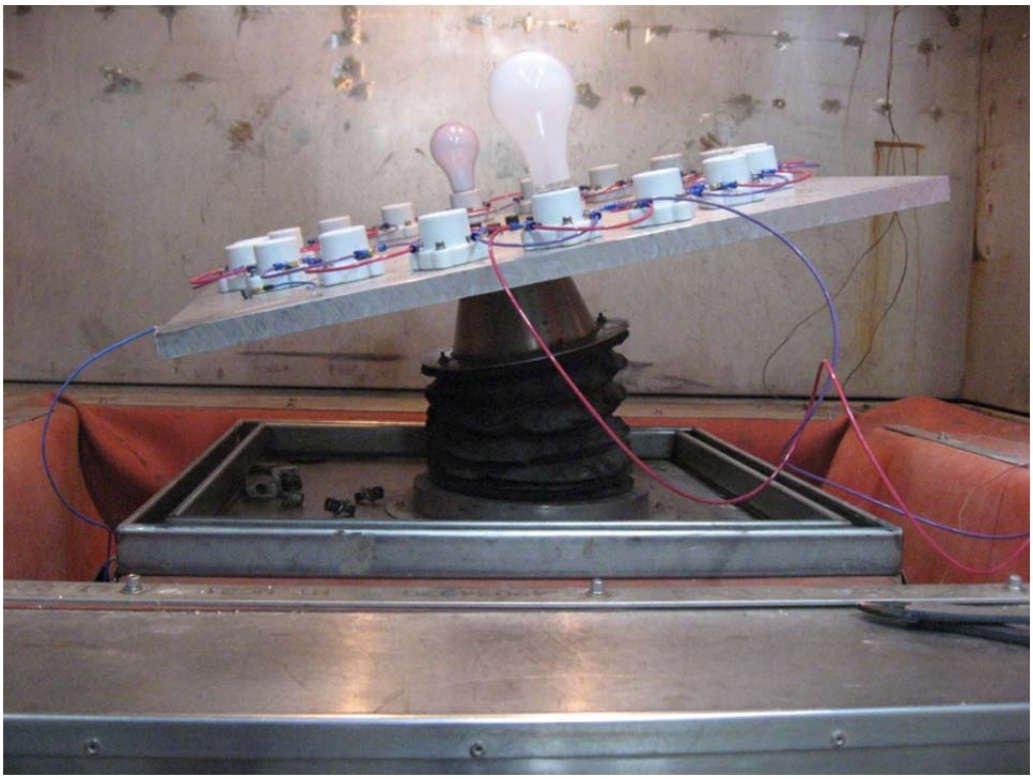

Figure 2.2. Stress Test Board, Showing Mounting on Vibration Table Head

Figure 2.3. Environmental Chamber With Mounted Stress Test Board

In addition to visual monitoring for loss of lamp function, all test samples were subject to functional verification testing following each stress step. Illuminance can be easily and rapidly measured using simple, inexpensive handheld meters, which are also well-suited for minimizing test time. The functional verification test setup was designed around the idea of using of a slightly more expensive, but similarly easy to use and convenient, handheld meter capable of simultaneously measuring illuminance and chromaticity. Because illuminance is only measured for a given surface, it is an appropriate metric for a directional lamp; however, it is less suitable for a omnidirectional source meeting L Prize requirements for replacing the common 60W incandescent A-lamp.

Although an omnidirectional light source can be reliably measured by mounting a sample in an integrating sphere, such an approach is prohibitively time-consuming. Instead, a downlight was used to approximate an integrating sphere, which allowed for measurement of light output from an omnidirectional source and rapid lamp mounting. After careful consideration of a variety of specification-grade makes and models, 6 in. aluminum downlights from Lithonia Lighting with clear semi-specular open reflectors were selected, based in large part on the strength of an optical design that maximizes lumen output. The selected luminaires were not the least expensive option, but their relatively low cost did allow for the design of a test setup with a dedicated downlight for each test sample, which facilitated a rapid transition from the environmental chamber to the powered functional verification environment, with negligible differences in power-down time between samples.

The functional verification test setup consisted of a measurement chamber, 18 downlights mounted to a custom-built chassis, and an illuminance/color meter (Figure 2.4). The downlight chassis was designed to position each luminaire equidistant from a table supporting the measurement chamber at a convenient working height (Figure 2.5). The measurement chamber was fabricated by painting a wooden, 24 in.

cubical box flat black inside and out, and cutting a hole 6 in. in diameter centered in the top of the box for interfacing with an overhead mounted downlight containing a test sample (Figure 2.6). A foam ring was attached to the hole to aid in alignment of the movable measurement chamber and to block ambient light (Figure 2.7). As is typical for such luminaires, the downlight reflector housing was mechanically attached to the box frame by multiple spring arms. The housing was seated by pressing it up into the arms, typically until the reflector trim ring was flush with the ceiling. The design allows for about 2 in. of positioning flexibility to accommodate different recessed ceiling thicknesses. The ability to vary the vertical positioning of the reflector housing facilitated rapid movement of the measurement chamber from one downlight to the next. Nominally, all reflector housings were pushed up to their highest vertical position. Prior to functional verification of a given test sample, the measurement chamber opening was aligned to the downlight and the reflector housing was lowered until it mated to the foam ring.

Measurements were taken using the illuminance/color meter at four locations on the bottom of the box, equidistant from the center (Figure 2.8). Alignment pins were inserted at all four locations to facilitate the rapid, repeatable positioning of the remote meter head for each measurement. Following transfer from the environmental chamber to the functional verification test setup and electrical connection, all lamps were allowed to stabilize for a minimum of 30 minutes before measurements were taken.

Figure 2.4. Functional Verification Test Setup

Figure 2.5. Downlight Chassis

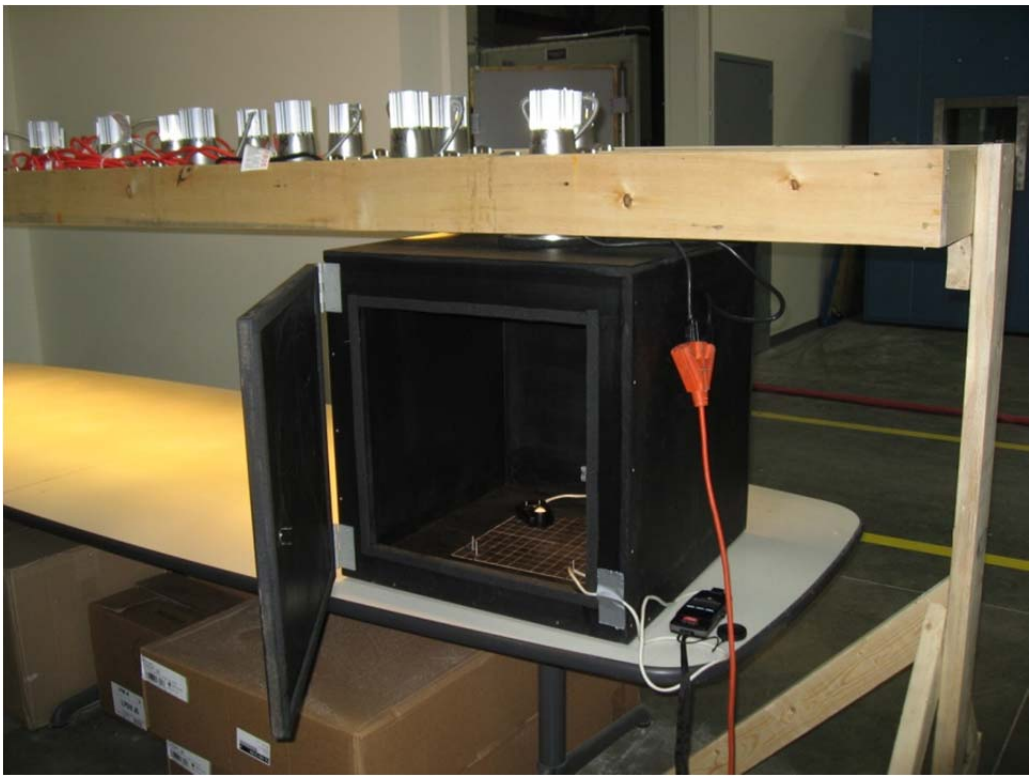

Figure 2.6. Measurement Chamber

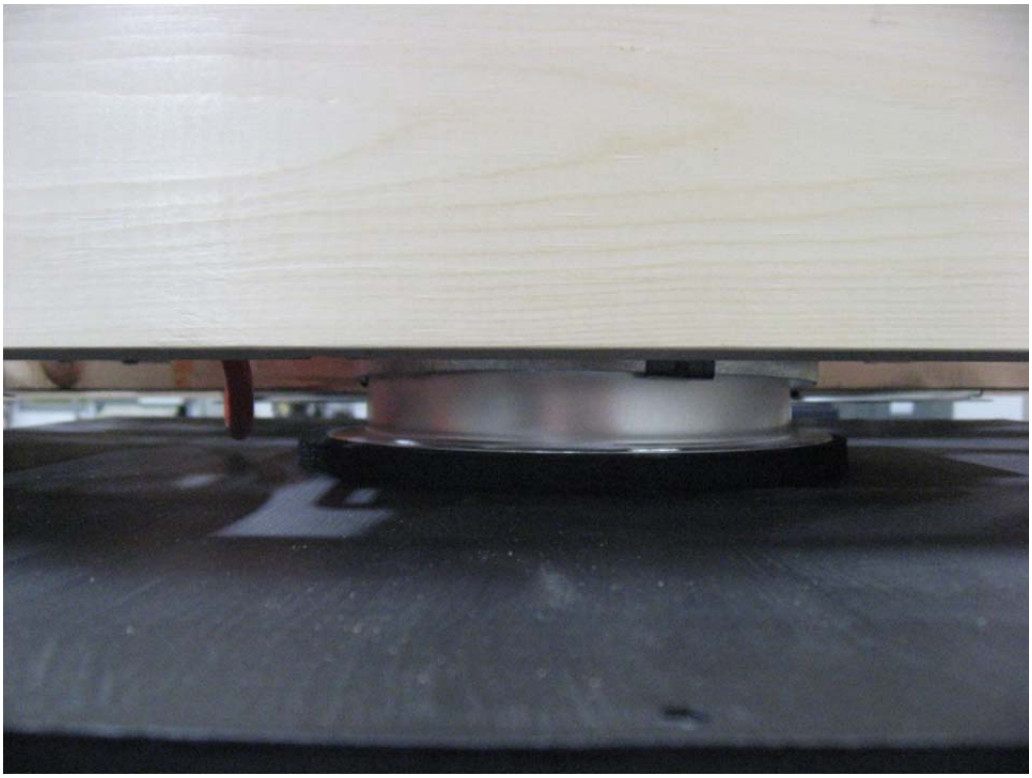

Figure 2.7. Foam Seal Mated to Downlight on Top of Measurement Chamber

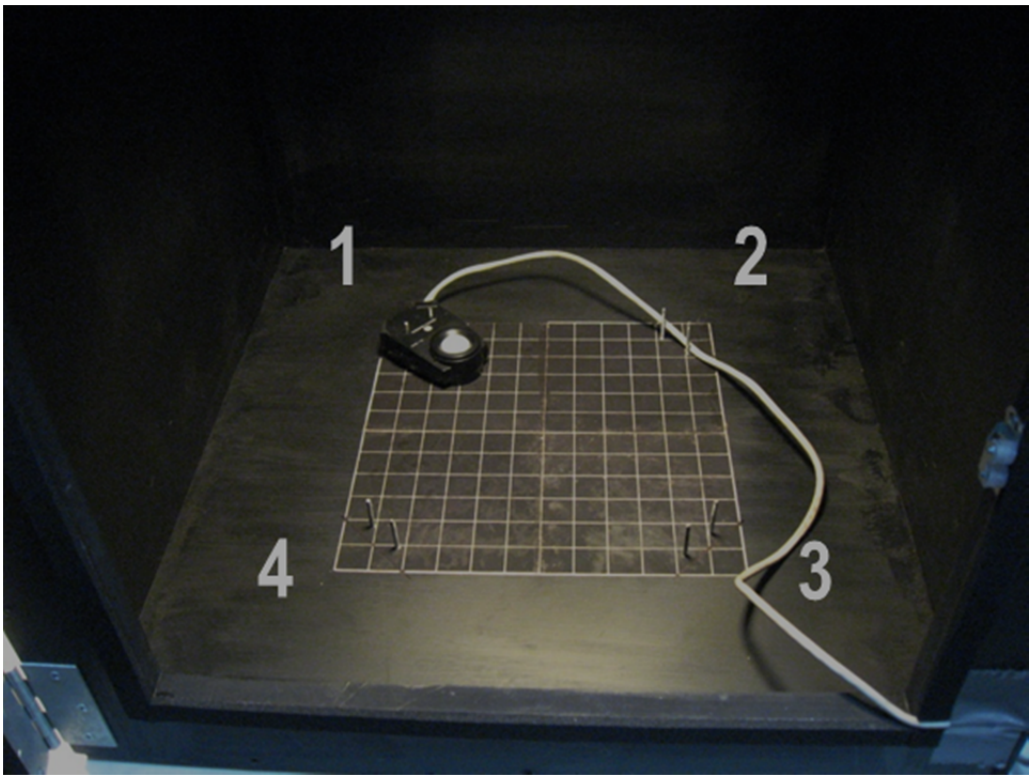

Figure 2.8. Illuminance/Color Meter Remote Head in the First of Four Measurement Locations

2.2 Test Plan

A 10-step preliminary test plan was developed based on the estimates of service (step 1) and destruct (step 10) levels for each stress source (Table 2.2). Note that neither relative nor absolute humidity set points are present in the test plan because, as mentioned previously, the test setup is incapable of measuring humidity. Consequently, control is limited to the ability to simply introduce humidity at a fixed rate during the hot temperature cycles of a step, if specified. Each step contained three temperature periods, in a hot/cold/hot sequence, to facilitate exposure to both the maximum hot-to-cold, and cold-to-hot transition stresses. The duration of each temperature setting was 40 minutes, resulting in a total stress step duration of 120 minutes, thereby leaving a little over 60 minutes for functional verification in between each stress step within the 30 hour stress test budget.

The temperature, vibration, and humidity stress profiles designed for all 10 steps are graphically depicted in Figure 2.9, and the voltage stress profile is similarly shown in Figure 2.10. Vibration and temperature were ramped up to their (initial) set points over a 5 minute time span. Subsequent temperature transitions were driven to occur within 10 minutes. Humidity was introduced to the environment chamber during the first hot cycle only. Operating voltage was oscillated between a high and low set point during the first 10 minutes of a temperature cycle at 1 minute intervals. For the next 30 minutes of a given temperature cycle, a 1 minute off-state period was inserted in between each high and low set point period. Note that the voltage profile is only plotted for the first 40 minutes (or one temperature cycle) of a given step; this same profile is repeated 3 times (once for each temperature period) over the course of each step.

Table 2.2. Preliminary Test Plan

Step	Time (Minutes) H = Hot C = Cold	Hot Temp (°C)	Cold Temp (°C)	Vibration (Peak g)	High Temp Humidity	Low Voltage	High Voltage	Total Harmonic Distortion
1	40 H + 40 C + 40 H	50.0	-20.0	5.0	Yes	114	126	Sine
2	40 H + 40 C + 40 H	56.7	-24.4	8.3	Yes	108	132	Sine
3	40 H + 40 C + 40 H	63.3	-28.9	11.7	Yes	102	138	Sine
4	40 H + 40 C + 40 H	70.0	-33.3	15.0	Yes	96	144	Sine
5	40 H + 40 C + 40 H	76.7	-37.8	18.3	Yes	90	150	Sine
6	40 H + 40 C + 40 H	83.3	-42.2	21.7	Yes	78	162	Sine +10%
7	40 H + 40 C + 40 H	90.0	-46.7	25.0	Yes	66	174	Sine +20%
8	40 H + 40 C + 40 H	96.7	-51.1	28.3	Yes	54	186	Square
9	40 H + 40 C + 40 H	103.3	-55.6	31.7	Yes	42	198	Square
10	40 H + 40 C + 40 H	110	-60.0	35.0	Yes	30	210	Square

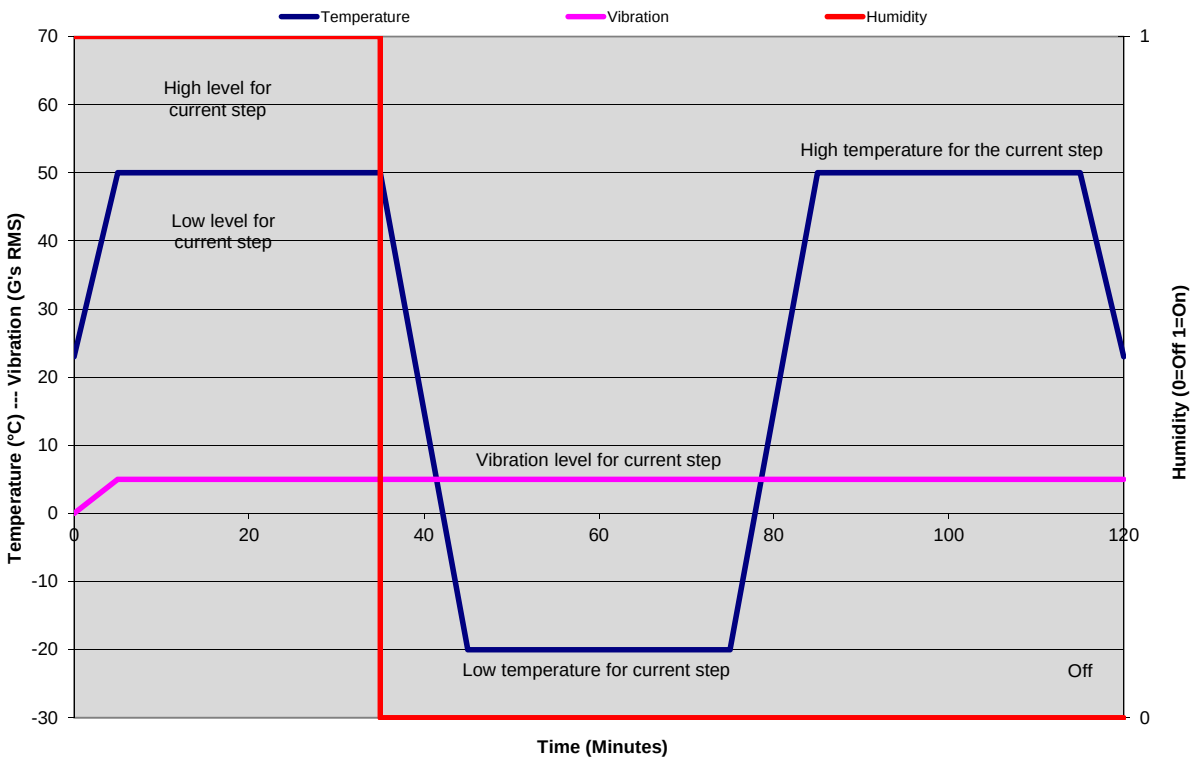

Figure 2.9. Temperature, Vibration, and Humidity Stress Profiles

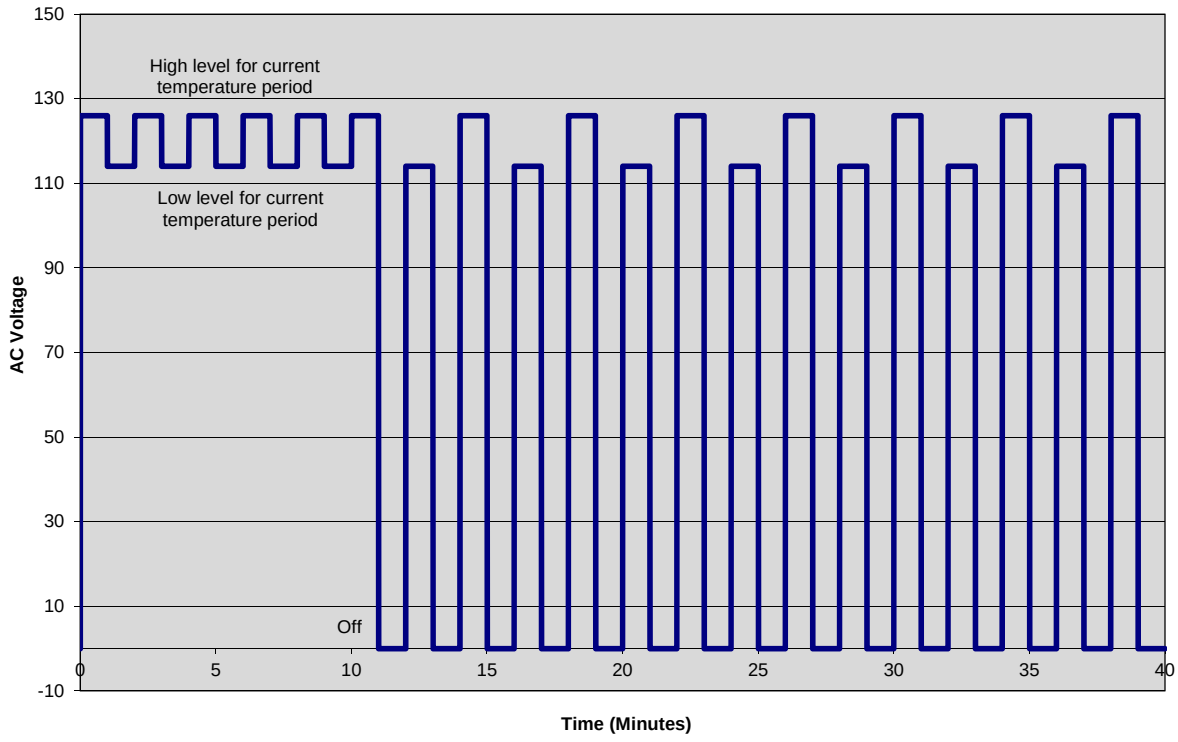

Figure 2.10. Voltage Stress Profile

2.3 Test Samples

Home Depot and Lowes provided the makes and models of their best-selling 60W incandescent replacement products. Using that information, three different compact fluorescent lamps (CFLs) were selected as benchmarks for comparison (Table 2.3). These samples are presumed representative of reliable CFLs based on their market success. Multiple samples of each make and model were procured from at least three different stores in the Portland, Oregon area.

Table 2.3. Benchmark CFL Test Samples

Sample Code	Make	Model
E	Ecosmart[(a)]	ES5M8144, 14W soft white
P	Philips	636219 (SKU) 227827 (model), 13W soft white
B	Bright Effects[(b)]	252003 (item) 017801997323 (model), 13W soft white

(a) Home Depot's store brand, manufactured by TCP
(b) Lowe's store brand, manufactured by General Electric, Feit, and others

Prior to testing, 15 Philips L Prize entry lamps and 15 benchmark CFLs (5 of each make and model) were subjected to absolute photometry testing (L Prize entry lamps per IES LM-79, CFLs per IES LM-66) in an integrating sphere; results are summarized in Table 2.4. The photometered Philips L Prize entry sample set contained lamps delivered by Philips in two separate batches, differentiated only by the insertion of phosphor panel retaining rings on the latter batch to compensate for a recently discovered error made by the subcontracted panel manufacturer. The initial set of test samples consisted of 9 Philips L Prize entry lamps (all with retaining rings) and 9 benchmark CFLs (3 of each make and model), randomly selected from the photometered pool, and shown in Figure 2.11 just prior to the initiation of stress testing.

Table 2.4. Test Sample Initial Performance

	Philips L Prize Entry samples		Benchmark CFL samples	
Parameter	Average	Std. Dev.	Average	Std. Dev.
Current (mA)	83.9	0.596	194.0	7.285
Power (Watts)	9.77	0.063	13.63	0.551
Power Factor	0.970	0.001	0.586	0.005
Current THD (%)	18.7	0.219	112.0	3.572
Luminous Flux (Lumens)	911.4	15.60	918.9	59.62
Efficacy (Lumens/Watt)	93.33	1.522	67.40	2.661
CCT	2718	17.94	2697	61.45
CRI	93.30	0.306	83.07	0.601
x-Chromaticity	0.459	0.00085	0.463	0.00387
y-Chromaticity	0.412	0.00072	0.415	0.00231

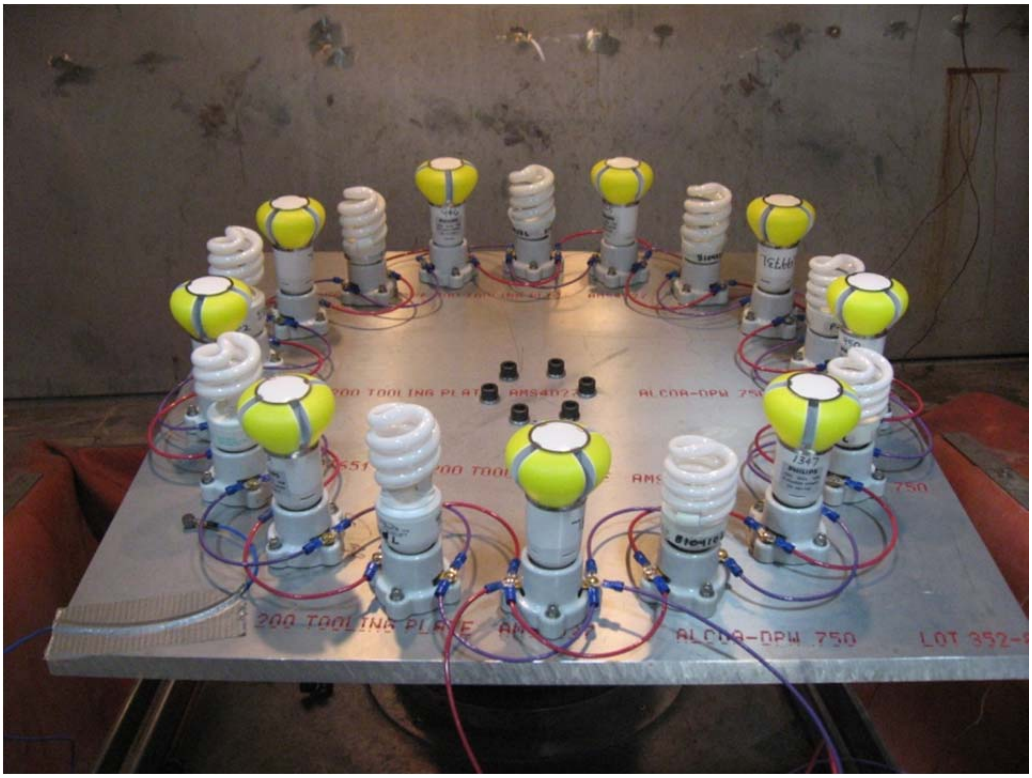

Figure 2.11. Initial Set of Test Samples Mounted on Test Board

3.0 Stress Testing

Following electrical verification of the test setup (Figure 3.1), stress testing commenced according to the preliminary test plan. All samples were visually observed during each test step, and failures were noted and verified at the completion of each test step. Samples that survived a given step were transferred to the functional verification test station for measurement. Samples that did not survive were removed from the test sample set, and replaced with a fresh sample from the remaining pool of photometered lamps prior to commencement of the next stress step.

Figure 3.1. Energized Test Board Prior to Stress Exposure

After finding no failed L Prize entry lamps following the completion of step 10, additional test steps (11.1, 11.2, 11.3, and 11.4; Table 3.1) were added a in an attempt to drive at least one L Prize entry lamp to failure. Temperature, vibration, and electrical stresses were incremented in each added step at a rate similar to that implemented in the preliminary test plan, but total stress duration was reduced by eliminating one or more temperature periods due to time constraints. Stress testing ceased following the completion of step 11.4, by which all CFL samples remaining on the test board had been driven to failure. Despite exposure to maximum temperature stresses of +137°C and -68.9°C, maximum vibrational stresses of 53.3 peak g, and maximum electrical stresses of 1 minute oscillations between off (0 V) and 258 VAC driven by a square wave, all L Prize entry lamps remained illuminated throughout testing (Figure 3.2).

Table 3.1. Final Test Schedule

Step	Time (Minutes) H = Hot C = Cold	Hot Temp (°C)	Cold Temp (°C)	Vibration (Peak g)	High Temp Humidity	Low Voltage	High Voltage	Total Harmonic Distortion
1	40 H + 40 C + 40 H	50.0	-20.0	5.0	Yes	114	126	Sine
2	40 H + 40 C + 40 H	56.7	-24.4	8.3	Yes	108	132	Sine
3	40 H + 40 C + 40 H	63.3	-28.9	11.7	Yes	102	138	Sine
4	40 H + 40 C + 40 H	70.0	-33.3	15.0	Yes	96	144	Sine
5	40 H + 40 C + 40 H	76.7	-37.8	18.3	Yes	90	150	Sine
6	40 H + 40 C + 40 H	83.3	-42.2	21.7	Yes	78	162	Sine +10%
7	40 H + 40 C + 40 H	90.0	-46.7	25.0	Yes	66	174	Sine +20%
8	40 H + 40 C + 40 H	96.7	-51.1	28.3	Yes	54	186	Square
9	40 H + 40 C + 40 H	103.3	-55.6	31.7	Yes	42	198	Square
10	40 H + 40 C + 40 H	110	-60.0	35.0	Yes	30	210	Square
11.1	40 H + 40 C	116.7	-64.4	38.3	Yes	18	222	Square
11.2	40 H	123.3	N/A	41.7	Yes	6	234	Square
11.3	40 H + 40 C	130.0	-68.9	50.5	Yes	0	246	Square
11.4	40 H	136.7	N/A	53.3	Yes	0	258	Square

Figure 3.2. Energized Test Board Following Completion of All Test Steps

3.1 Test Sample Failure Progression

Table 3.2 shows the complete test board sample history. Each lamp socket on the test board was assigned a number, and the lamp sample number seated in each position was recorded prior to the commencement of each stress step. L Prize entry lamps had four digit numerical codes; CFL benchmarks were coded according to their make and model (E, P, B from Table 2.3) and purchase location. Following the completion of each stress step, failed lamps were noted by color coding the lamp number (e.g., three CFL samples failed during step 6: B-1-1 in lamp position 11, P-3-1 in lamp position 17, and P-2-1 in lamp position 18). As previously mentioned, failed lamps were replaced by fresh samples prior to the commencement of the subsequent stress step (e.g., following the completion of step 7, failed lamp P-1-2 in lamp position 16 was replaced by sample E-1-1, which in turn failed during stress step 8, prompting its replacement with L Prize entry sample 0530. Note that all four additional stress cycles were treated as one stress step; the results following the final cycle (11.4) are recorded in the test board sample history as stress step 11.

Table 3.2. Test Board Sample History

Lamp Position	Stress Step										
	One	Two	Three	Four	Five	Six	Seven	Eight	Nine	Ten	Eleven
1	**0948**	**0948**	**0948**	**0948**	**0948**	**0948**	**0948**	**0948**	**0948**	**0948**	**0948**
2	**1229**	**1229**	**1229**	**1229**	**1229**	**1229**	**1229**	**1229**	**1229**	**1229**	**1229**
3	**0949**	**0949**	**0949**	**0949**	**0949**	**0949**	**0949**	**0949**	**0949**	**0949**	**0949**
4	**1375**	**1375**	**1375**	**1375**	**1375**	**1375**	**1375**	**1375**	**1375**	**1375**	**1375**
5	**0946**	**0946**	**0946**	**0946**	**0946**	**0946**	**0946**	**0946**	**0946**	**0946**	**0946**
6	**1225**	**1225**	**1225**	**1225**	**1225**	**1225**	**1225**	**1225**	**1225**	**1225**	**1225**
7	**1266**	**1266**	**1266**	**1266**	**1266**	**1266**	**1266**	**1266**	**1266**	**1266**	**1266**
8	**0950**	**0950**	**0950**	**0950**	**0950**	**0950**	**0950**	**0950**	**0950**	**0950**	**0950**
9	**1347**	**1347**	**1347**	**1347**	**1347**	**1347**	**1347**	**1347**	**1347**	**1347**	**1347**
10	B-2-1	B-2-1	B-2-1	B-2-1	B-2-1	B-2-1	B-2-1	B-2-1	B-2-1	B-2-1	B-2-1
11	B-1-1	B-1-1	B-1-1	B-1-1	B-1-1	B-1-1	B-3-1	B-3-1	B-3-1	B-3-1	B-3-1
12	B-2-2	B-2-2	B-2-2	B-2-2	B-2-2	B-2-2	B-2-2	B-2-2	B-2-2	B-2-2	B-2-2
13	E-3-1	E-3-1	E-3-1	E-3-1	E-3-1	E-3-1	E-3-1	E-3-1	**0534**	**0534**	**0534**
14	E-2-2	E-2-2	E-2-2	E-2-2	E-2-2	E-2-2	E-2-2	E-2-2	E-2-2	E-2-2	E-2-2
15	E-1-2	E-1-2	E-1-2	E-1-2	E-1-2	E-1-2	E-1-2	E-1-2	E-1-2	E-1-2	E-1-2
16	P-1-2	P-1-2	P-1-2	P-1-2	P-1-2	P-1-2	P-1-2	E-1-1	**0530**	**0530**	**0530**
17	P-3-1	P-3-1	P-3-1	P-3-1	P-3-1	P-3-1	P-1-1	E-2-1	**0531**	**0531**	**0531**
18	P-2-1	P-2-1	P-2-1	P-2-1	P-2-1	P-2-1	P-4-1	E-4-1	E-4-1	**0532**	**0532**

Bold = Philips L Prize entry; Red = failure step

3.2 Functional Verification

Test samples that continued to provide visible light following the completion of each stress step were transferred to the functional verification test setup and further examined through measurements of illuminance and chromaticity. Average relative (normalized) illuminance measurements for all tested Philips L Prize entry samples, following the completion of each stress step, are charted in Figure 3.3. Similarly, illuminance measurements for the CFL samples are shown in Figure 3.4, Figure 3.5 and Figure 3.6 show Δx chomaticity results and Figure 3.7 and Figure 3.8 show Δy chromaticy results. In all

plots, lamp failure for a give sample is noted by recording a 0 for average illuminance, and a -1 for average Δx or Δy chromaticity coordinate.

The average illuminance measurements for the Philips L Prize entry samples remained within ±10% of their initial pre-test measurements over the course of all stress steps, with the exception of one sample (0530) which fell below this band following the completion of stress step eleven (Figure 3.3). The CFL counterparts maintained a similarly tight distribution over the first five stress steps, but samples began failing or showing consistently degrading illuminance thereafter (Figure 3.4). Chromaticity measurements of all samples showed almost no deviation from their initial pre-test measurements up to the point where the sample failed. Again, the Philips L Prize entry sample 0530 was the exception. As noted in Table 3.2, sample 0530 was not one of the initial 9 test samples, but rather one of the backups from the pool of 15 photometered lamps; it was substituted into lamp position 16 prior to the commencement of step 9 after the pool of photometered CFL samples had been exhausted. Sample 0530 did not have the aforementioned phosphor panel retaining rings (shown in Figure 3.9), and during the additional test steps, one of the phosphor panels became dislodged. Functional verification testing for this sample was consequently done without the phosphor panel, which accounts for both the exhibited reduction in illuminance and chromaticity shifts.

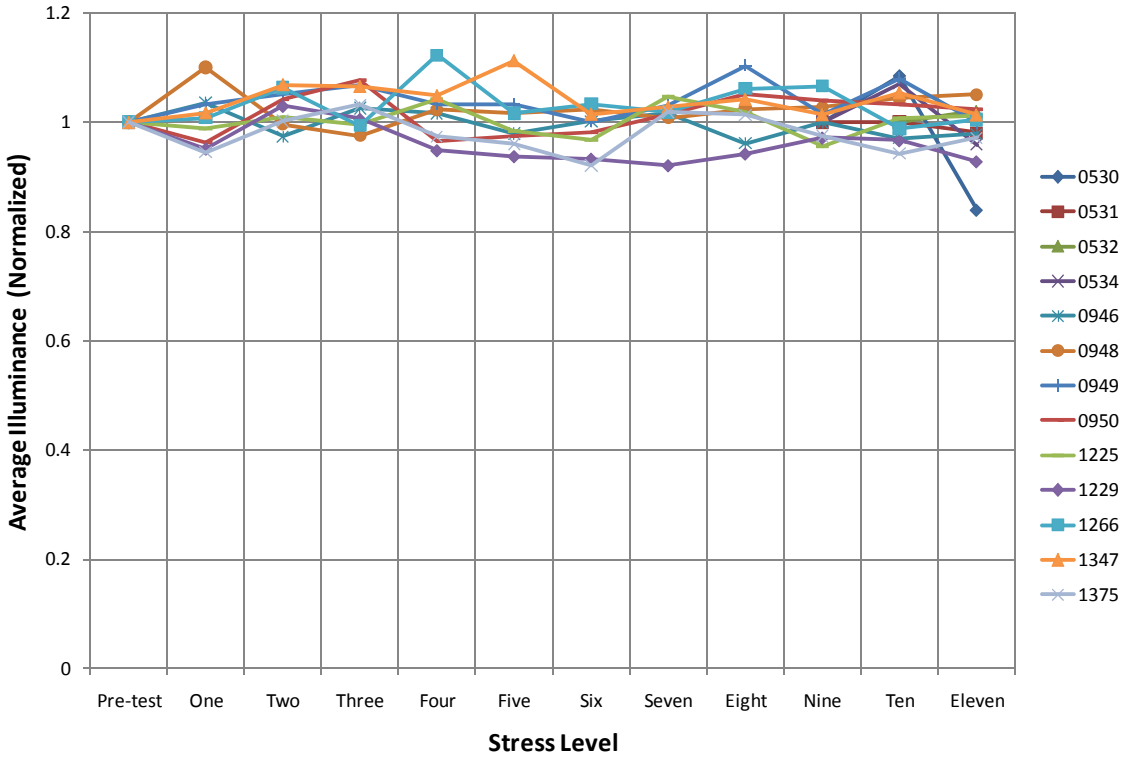

Figure 3.3. Philips L Prize Entry Illuminance Results

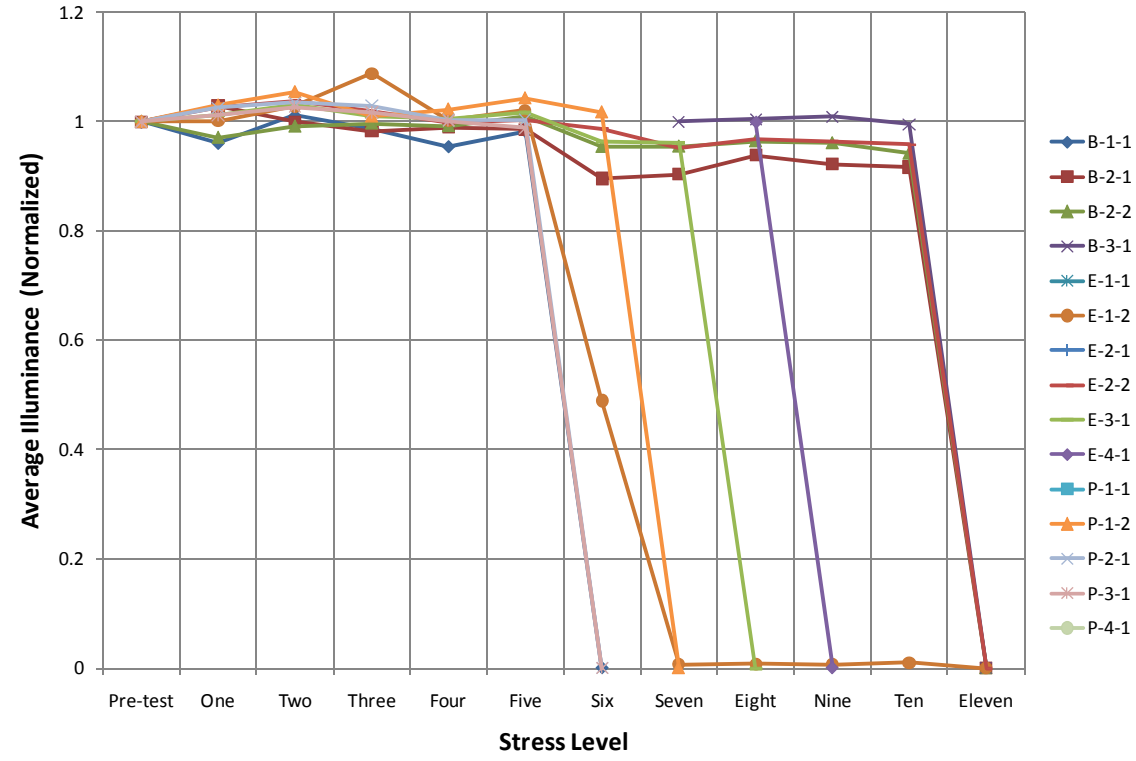

Figure 3.4. CFL Illuminance Results

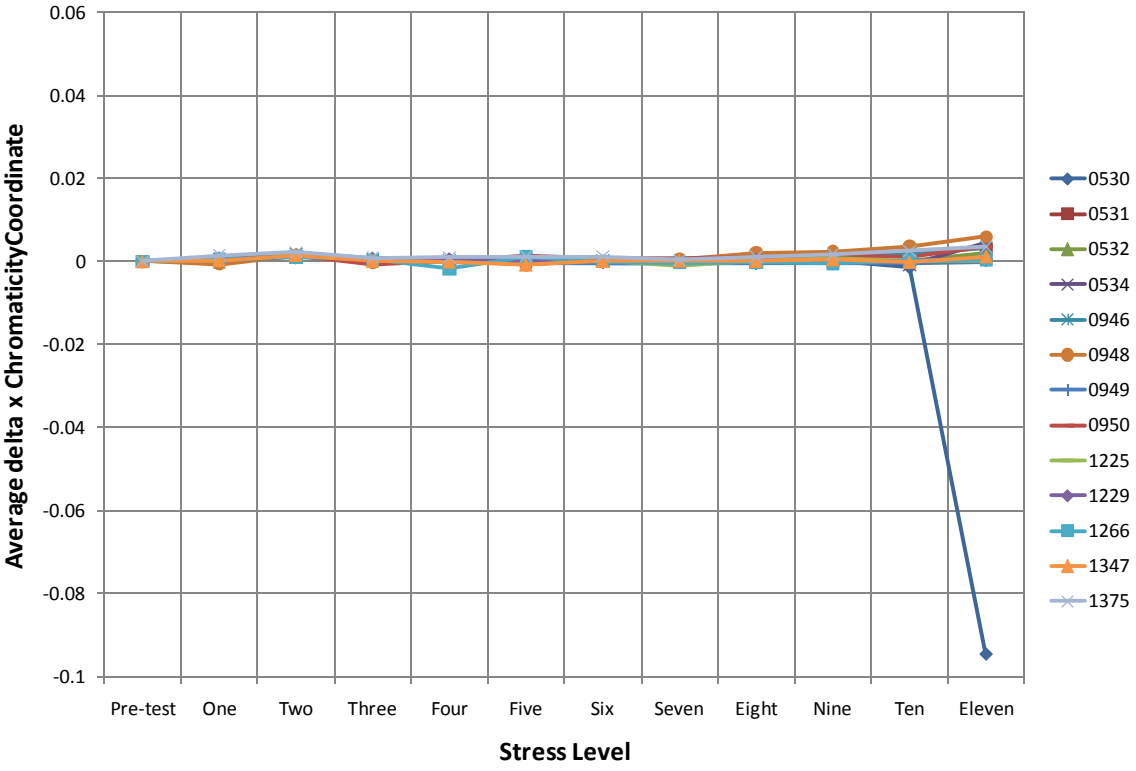

Figure 3.5. Philips L Prize Entry Δx Chromaticity Results

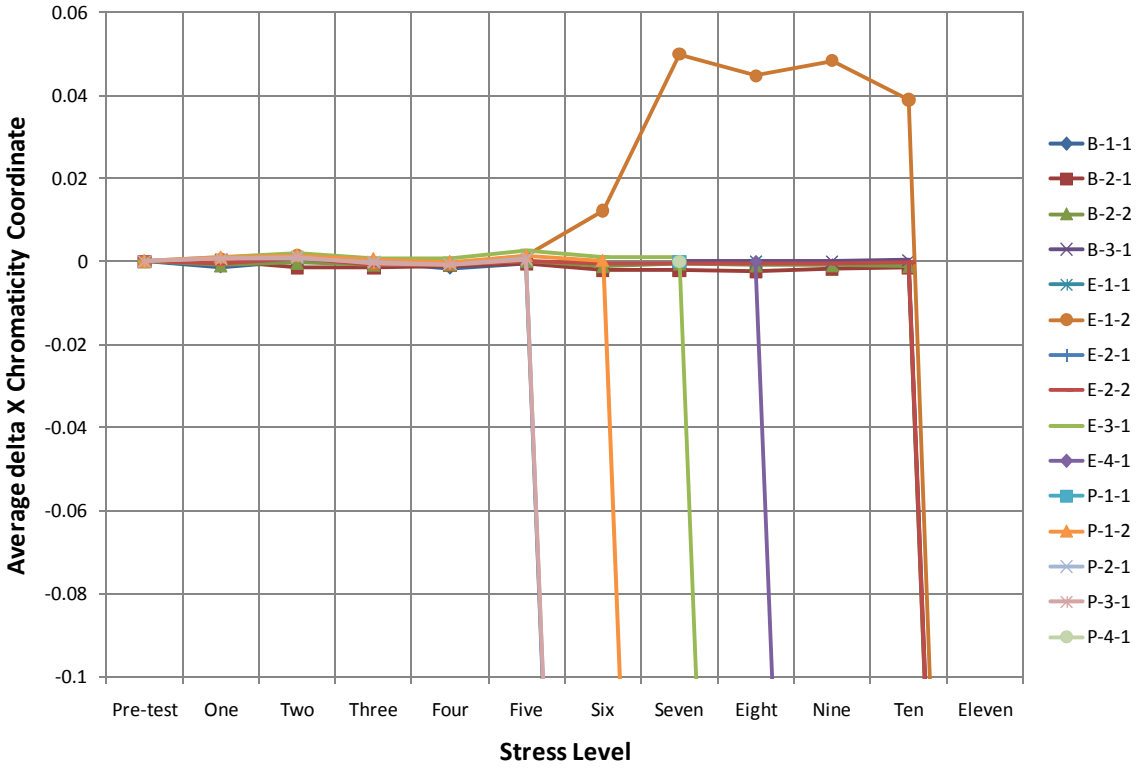

Figure 3.6. CFL Δx Chromaticity Results

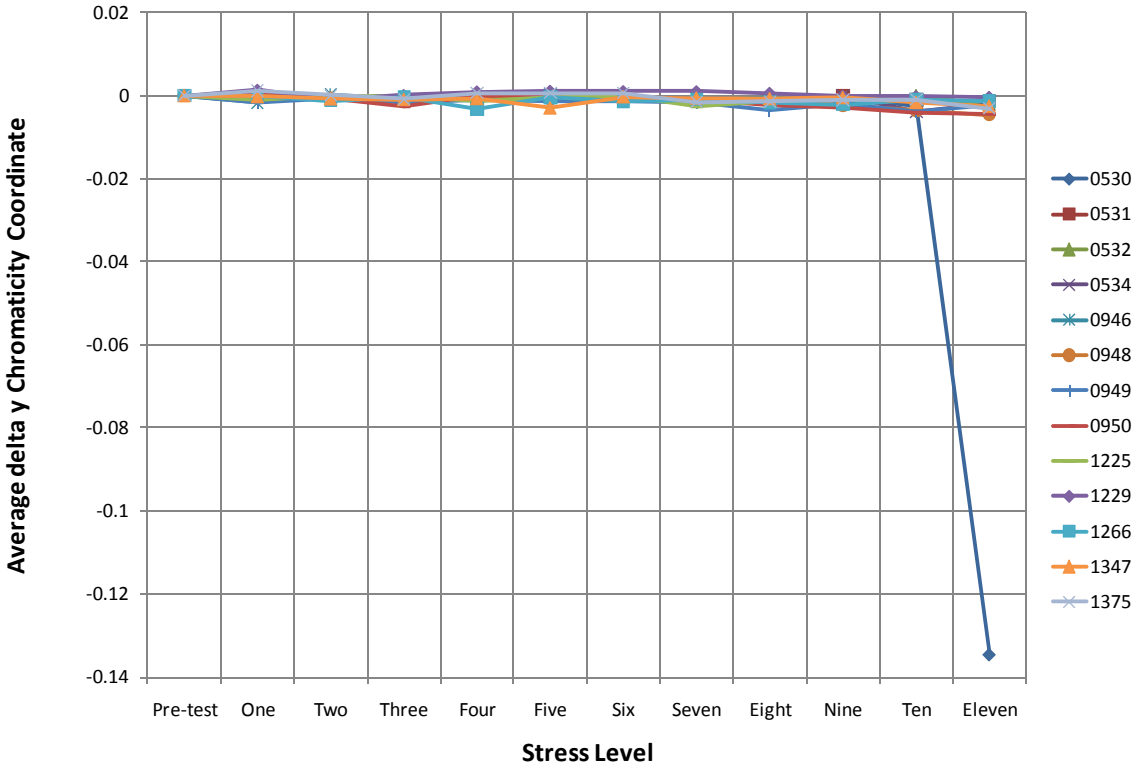

Figure 3.7. Philips L Prize Entry Δy Chromaticity Results

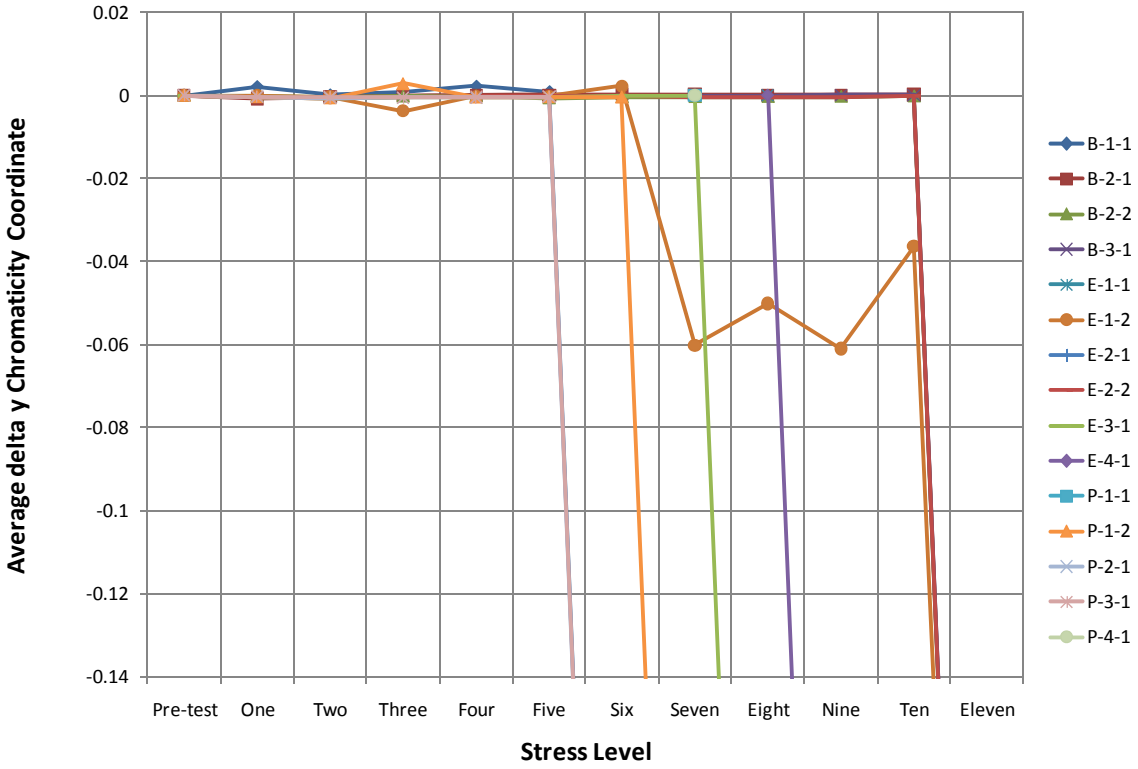

Figure 3.8. CFL Δy Chromaticity Results

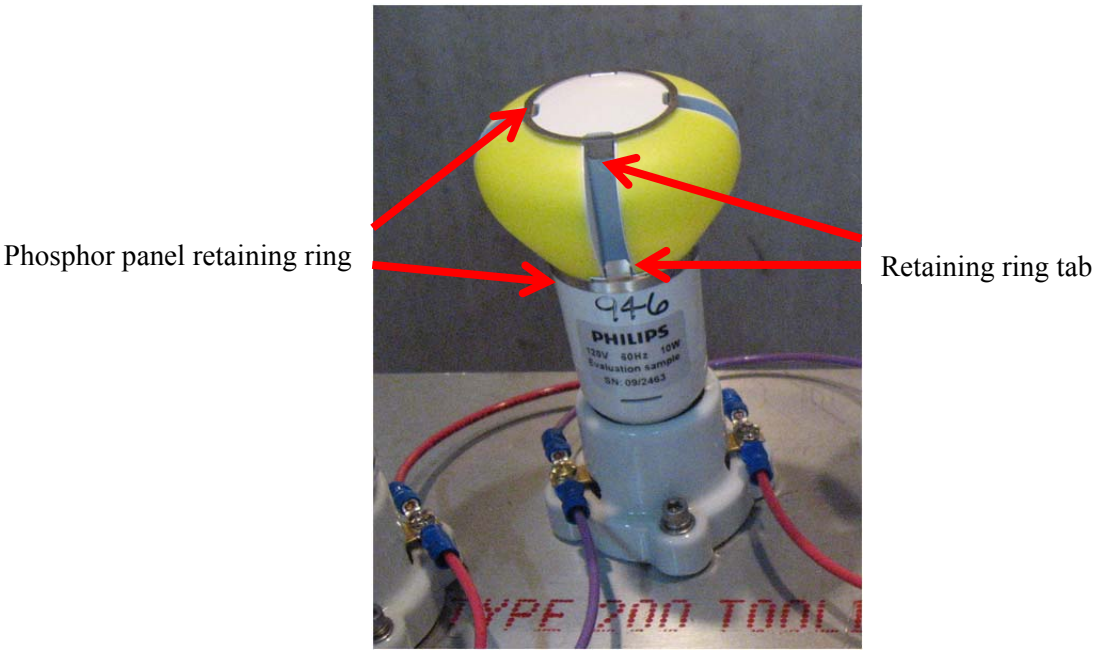

Figure 3.9. Philips L Prize Entry Close-Up View, Showing Phosphor Panel Retaining Ring

4.0 Post-Stress Analysis

Once stress testing was completed, failed samples were examined in an attempt to identify unique failure modes, and a basic failure progression analysis was performed to explore the design maturity and technology limit for the benchmark CFL and the competing Philip L Prize designs.

4.1 Failure Modes

Failed test samples were first visually inspected for exterior signs of damage. Fresh, un-tested samples of each lamp make and model were used to determine the most efficient non-destructive method for performing an interior inspection. Once access to interior components was gained, failed samples were visually inspected again, this time with a focus on solder joint failures, heat damage, and obvious destruction of electronic components (e.g., electrolytic capacitors).

4.1.1 Benchmark CFL Analysis

Exterior examination of the failed benchmark CFLs revealed little damage or degradation, other than the apparent softening of the sealant used to attach spiral fluorescent tube to lamp base noted on some samples. The softening was significant enough to allow for the relatively easy removal of the spiral tube from one sample, which facilitated investigation of whether the fluorescent tube had failed, or the ballast in the base. The two halves of a fresh, un-tested sample were carefully separated, and the wires connecting the ballast to the fluorescent electrodes were cut, allowing the ballast to be connected to the spiral tube from the failed sample. The newly constructed sample lit when power was applied, strongly suggesting that the failed sample has ceased to operate due to ballast damage.

Interior access to all CFL samples was achieved by prying open a snap-fitting at the seam, as shown in Figure 4.1. Visual inspection did not reveal any obvious solder joint failures or heat damage. Electrical continuity testing was done across resistors or through-hole connections where accessible, but again no clear failure points were discovered. The large electrolytic capacitor present in all CFL samples was carefully pried to its maximum extension and examined for ruptures and signs of heat damage (Figure 4.2); no evidence of either was found in the failed samples. Time did not allow for de-soldering components in the failed CFL samples to perform a more thorough investigation. In lieu of any additional insight provided by such an investigation, evidence suggested that ballast failure led to the demise of the CFL samples, but not due to a single failure point or component failure.

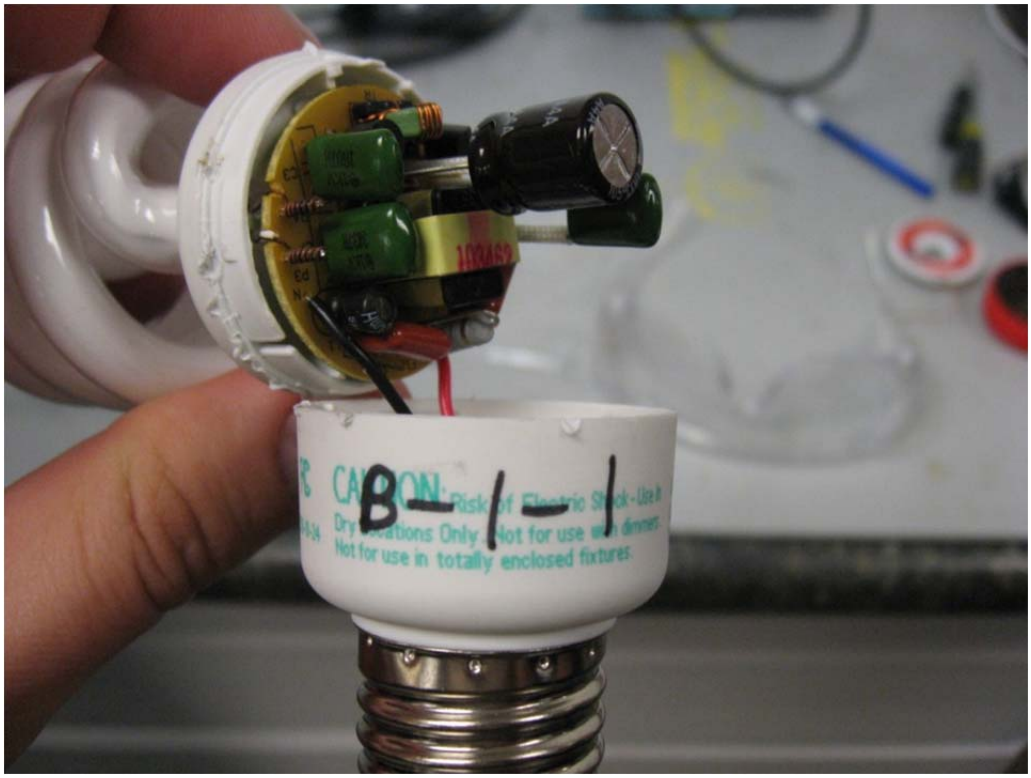

Figure 4.1. CFL Disassembly for Failure Analysis

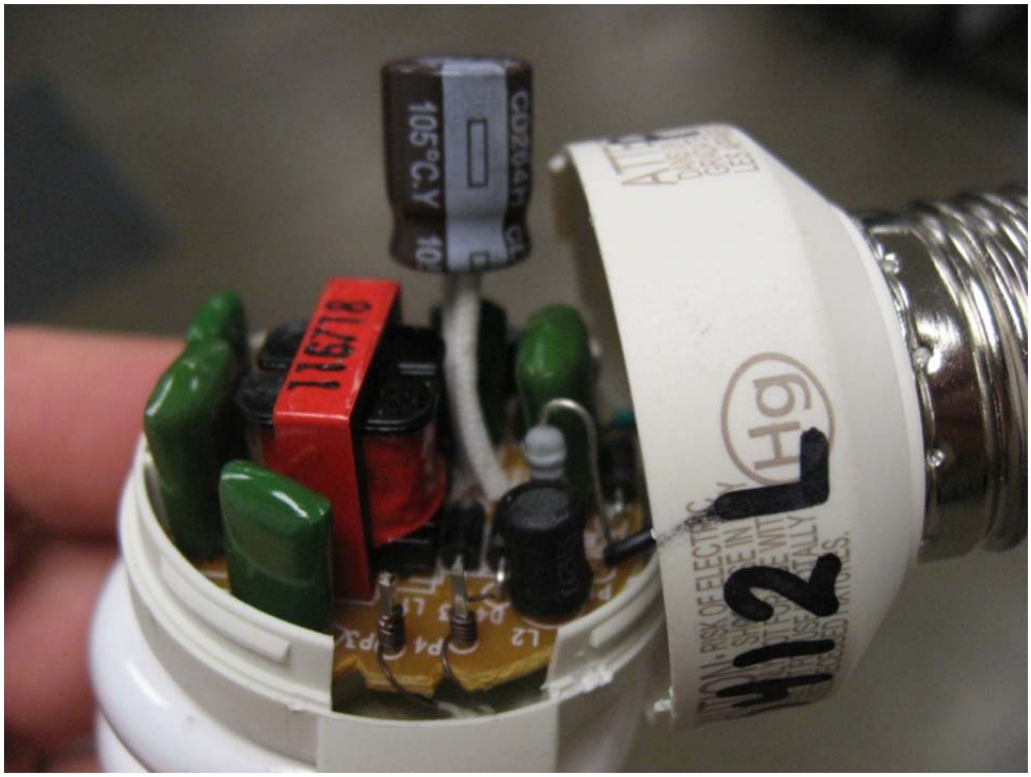

Figure 4.2. Examination of CFL Electrolytic Capacitor

4.1.2 Philips L Prize Entry Analysis

Due to the lack of any design-intent failures on the Philips L Prize entry lamps, no meaningful failure analysis could be done.

4.2 Failure Progression

The identification of unique failure modes and analysis of their occurrence over progressive stress testing can provide insight into a product's design maturity and its potential for improvement. Exploration of the design maturity of a number of similar products manufactured using a common technology may reveal the limits of the technology

4.2.1 Design Maturity

Design Maturity (DM) is a metric for the average potential for improvement in the design of a product that can be achieved by fixing one failure mode. The DM of a product is measured by conducting a FMVT and plotting the failure mode progression. DM quantifies the spread or distribution of individual failure modes in a product by calculating the ratio between the average time between failures after the first failure, and the first failure, according to Equation 4.1 (Intertek 2004).

$$DM = \frac{Tave}{Tmin} = \frac{(Tmax\text{-}Tmin)}{(Count\text{-}1) \times Tmin} \tag{4.1}$$

where Tmax = Time to the last unique failure found
Tmin = Time to the first unique failure found
Count = Number of unique failures found

Predicted values for DM (PDMi) can be calculated for design changes by which one or more of the earliest failure modes are corrected (Equation 4.2).

$$PDMi = \frac{(Tmax\text{-}T(i+1))}{(Count\text{-}1\text{-}i) \times T(i+1)} \tag{4.2}$$

where i = ith failure mode
Tmax = Time to the last unique failure found
T(i+1) = Time to the ith+1 unique failure found
Count = Number of unique failures found

A FMVT design plan, which aims to set stress levels progressing from service to destruct, is based on the presumption that a reliable product will accumulate stress damage over the course of testing in a uniform way, and failure modes will express themselves over a short period of time close to the destruct level (Intertek 2004), resulting in a failure mode progression of the form shown in Figure 4.3. If, however, a failure mechanism is accumulating damage faster than the rest of the design at or near service conditions, then that failure mechanism will express itself well before the rest of the design fails (Figure 4.4). Ideally, such weak failure mode(s) should be targeted for correction.

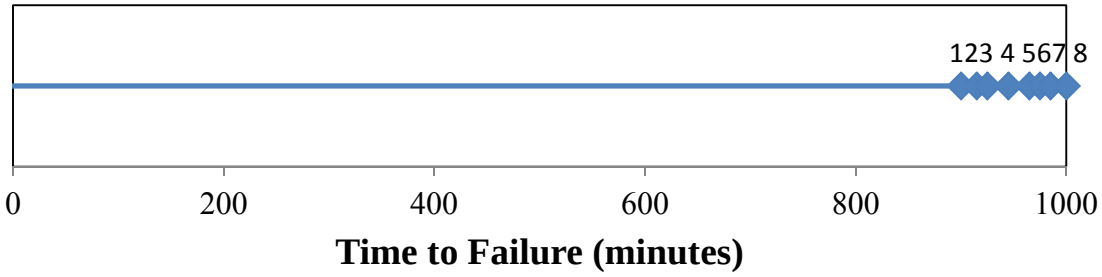

Figure 4.3. Example Failure Progression for a Highly Reliable Product (Intertek 2004)

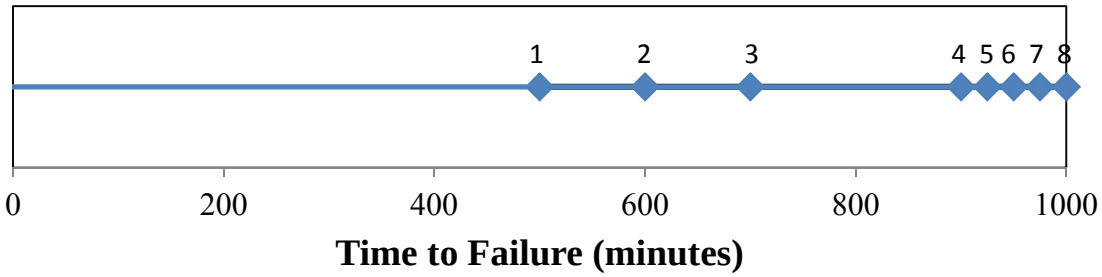

Figure 4.4. Example Failure Progression for a Product With a Weak Failure Mode (Intertek 2004)

4.2.2 Technology Limit

Highly reliable products have DM values close to zero, which indicates very little room for improvement. In the practice of using FMVT to examine the reliability of products, the technology limit has been empirically determined to be when DM = 0.1 (Intertek 2004). This axiom suggest that if DM > 0.1, failures should be fixed to bring the DM < 0.1, at which point the design cannot be reasonably made better without a fundamental change in its technology. The number of failure modes that need to be fixed to bring a design to its technology limit is thereby i such that PDMi < 0.1.

4.2.3 Benchmark CFL Analysis

A failure progression analysis starts with the identification of first occurrence of each unique failure mode. Only limited monitoring and failure analysis was done, so some assumptions have to be made:

1. Times to failure are known, but as described in Section 4.1, the exact failure modes for test samples that simply stopped emitting light are not easily discerned. Only the first occurrence of each unique failure is of interest, so each unique time to failure is assumed to be a unique failure.
2. All failures are assumed to have occurred at the very end of the step where the failure occurred.

An examination of the test board sample history (Table 3.1) using these assumptions leads to the following set of progressive failures:

1. The first failure mode occurred during step 6, affecting both B and P samples.

2. The second failure mode occurred during step 7, affecting not only the single remaining original P sample, but also the two newly inserted (following step 6) P samples.
3. The third failure mode occurred during step 8, affecting only E samples. The failure of E-4-1 during step 9 was assumed to be the result of the same failure mode, based on the multiple failures of E samples in step 8 and the lack of any other failures during step 9.
4. The fourth and final failure mode occurred during step 11, affecting all remaining CFL samples.

The benchmark CFL failure progression, summarized in Table 4.1 and plotted in Figure 4.5, allows for the calculation of DM (Equation 4.3), as well as the PDMi for correction of the first two failure modes (PDM_1 [Equation 4.4] and PDM_2 [Equation 4.5]). These results suggest that the CFL technology represented by the evaluated test samples is moderately mature. The calculated design maturity suggests room for design improvement (DM = 0.28 > 0.1). Correction of the first two observed failure modes does not result in a reduction of DM, however, suggesting that the observed failure modes represent the end-of-life cluster in a mature design.

$$DM = \frac{(1320 - 720)}{(4\text{-}1) \times 720} = 0.28 \tag{4.3}$$

$$PDM_1 = \frac{(1320 - 840)}{(4\text{-}1\text{-}1) \times 840} = 0.29 \tag{4.4}$$

$$PDM_2 = \frac{(1320 - 960)}{(4\text{-}1\text{-}2) \times 960} = 0.38 \tag{4.5}$$

Table 4.1. Benchmark CFL Failure Progression

Failure Number	Failure Description	Time Into Testing (minutes)
1	Failure Mode 1 (no light output)	720
2	Failure Mode 2 (no light output)	840
3	Failure Mode 4 (no light output)	960
4	Failure Mode 3 (no light output)	1,320

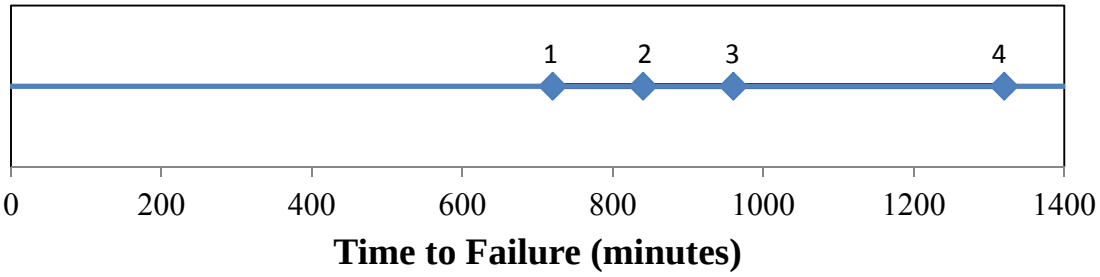

Figure 4.5. Benchmark CFL Failure Progression

4.2.4 Philips L Prize Entry Analysis

Due to the lack of any design-intent failures on the Philips L Prize entry lamps, no meaningful failure mode progression analysis could be done.

5.0 Suggestions for Additional Analysis and Future Testing

Possibilities for additional analysis of the existing data set are limited due to the lack of Philips L Prize entry failures, and the rapid (typically during one stress level) performance degradation (as measured by the defined functional verification tests) and lack of clearly unique failure modes exhibited by the benchmark CFL samples. Conversion of the x, y chromaticity measurements to other color spaces (u,v or u'v') may be worthwhile to facilitate easier interpretation of the relative color shift. More detailed failure mode analysis of the CFL samples might possibly reveal the failed electronic component(s).

The most obvious shortcoming of the completed testing was the inability to create failures in the Philips L Prize entry samples. Future testing should strive to expose one or more failure modes, by adjusting the stress levels and/or extending the available stress times. Given that the additional stress cycles were run at levels approaching the maximum capability of the existing test setup, the application of longer stress times may be necessary. Techniques for enhancing the damage potential of each stress type should be explored, including the introduction of particles and more complex electrical disturbances. Variations in the individual stress profiles and their combined effect should be reviewed to maximize combined impact. Finally, additional functional verification testing should be explored (e.g., measurement of input power, current, and power factor), in the hopes of observing more subtle or gradual performance degradation over stress periods.

6.0 References

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