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Noise Performance Evaluation of the Candidate Digitizers for the MAJORANA DEMONSTRATOR

E. Aguayo

March 2011

Pacific Northwest NATIONAL LABORATORY

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March 2011

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Executive Summary

The noise performance of the tow digitizer cards being considered for the MJD is presented. The procurement of the data acquisition electronics for the MJD is scheduled to happen this year. At the time of writing this document, there are two candidate digitizer electronic boards. The feasibility of using the demonstrator for dark matter is going to be dictated by the ability of the demonstrator to reach sub-kev energy resolution. One of the potential sources of noise is the data acquisition system. This document aims to help the decision of the final digitizer board by comparing the noise performance of the two electronic systems. A detailed description of the experimental data acquisition system set-up is presented. Noise parameters such as the effective number of bits, input range linearity and signal to noise ratio are experimentally determined. The two digitizer cards feature different on-board digital signal processing and these features are compared. The experimental set-up was also used to identify sources of noise. This paper describes these sources of noise in the data acquisition system, along with mitigation strategies. Issues such as grounding and wiring scheme have an impact in the overall data acquisition system performance and are discussed in detail. As a conclusion, the suitability of each one of the cards to become the back bone of the data acquisition system of the MJD is discussed.

Acronyms and Abbreviations

MJD	MAJORANA DEMONSTRATOR
HPGe	High Purity Germanium
PNNL	Pacific Northwest National Laboratory
LBNL	Lawrence Berkeley National Laboratory
DAQ	Data Acquisition System
GUI	Graphical User Interface
ORCA	Object-oriented Real-time Control and Acquisition
UNC	University of North Carolina
VME	VERSAmodule Eurocard
SBC	Single Board Computer
HV	High Voltage
ADC	Analog to Digital Converter
OS	Operating System
LSB	Less Significant Bits
ENOB	Effective Number Of Bits
GAT	Germanium Analysis Toolkit
GRETINA	Gamma Ray Energy Tracking In-beam Nuclear Array

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1 Introduction

The MJD is a low background experiment that has been designed to hold up to 40 Kg. of HPGe detectors. This detector mass will be divided into two arrays with an independent cryostat, with up to 35 detector channels per cryostat. The signal from these detectors will be digitized using state of the art electronics. Two are the options being considered by the MAJORANA collaboration; the Stuck 3302 manufactured by Struck Innovative Systeme [1] and a custom developed digitizer board developed at LBNL for the GRETINA [2] detector.

An experimental set-up for the evaluation of the two digitizer boards is described in this document. An experimental measure of the quality of the digitized signal is done calculating the ENOB for both cards. The measurement of both the differential and integral nonlinearity of the input stage will help in the decision of which card is more appropriate for a successful dark matter application of the experiment.

Both digitizer boards share the same VME64[3] backplane bus architecture, as well as coaxial input ports for the digitizers inputs. It was clear for the MAJORANA collaboration that the data bandwidth capabilities of parallel multidrop buses such as the VME bus will aid the data throughput performance in this data-intensive application. The potential drawbacks of using this type of system architecture are discussed in this document.

The whole data acquisition system will be software controlled using ORCA[4]. This data acquisition software has objects created to control each one of the candidate digitizer cards. A short introduction to these objects is presented. Each one of the digitizer cards features digital signal capabilities, slightly different form each other. Both cards use a digital filter to generate triggers, and they both have an embedded energy filter. These features are described and their expected performance when used in germanium detectors is discussed.

2 Experimental Set-up

The list of components for the experimentation with digitizers is similar to that used in spectrometry measurements. The experimentation presented in this document with the two cards was carried out at the University of North Carolina, during the winter of 2011. The principal elements of the experimental set-up were an experiment control computer with ORCA installed, a VME crate (including an SBC, HV source and digitizer boards) and a pulse generator. The initial experimentation was performed in Room 2 of Phillips Hall at UNC, but after identifying a number of noise sources in the room (cell phone signal, fluorescent lights, electronic equipment…) the whole set-up, as shown ion figure 1 was moved into a Faraday cage, located at Chapman Hall at UNC.

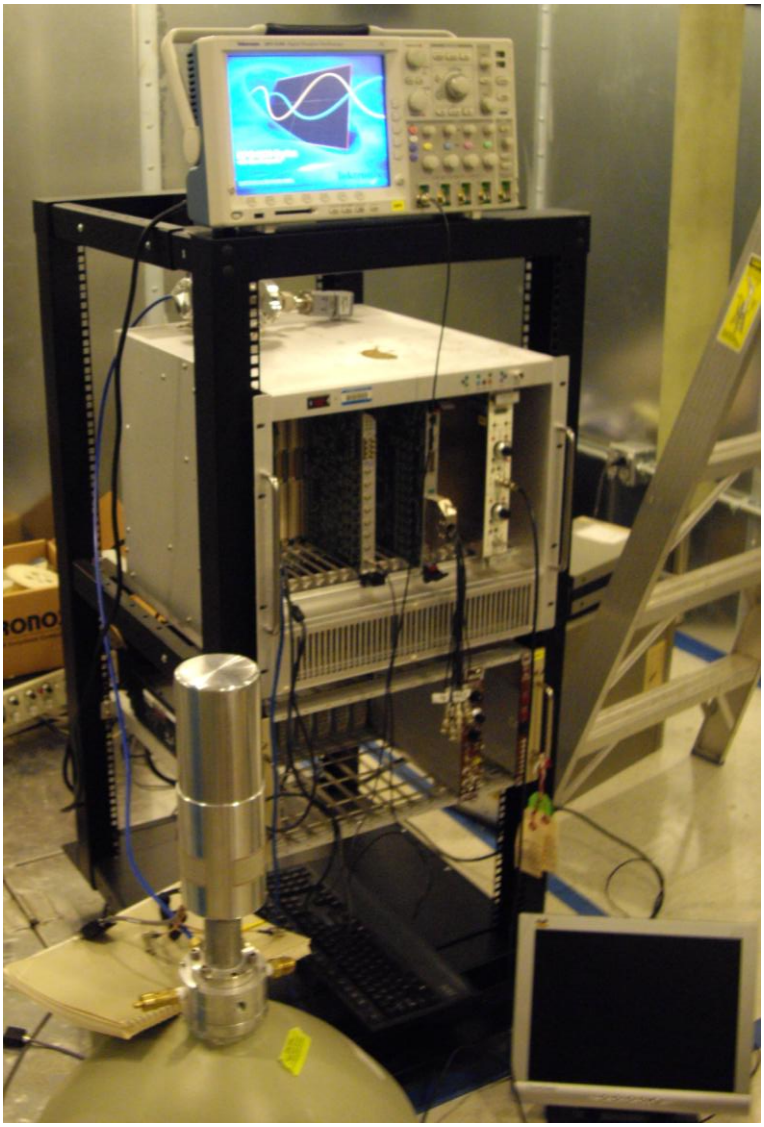

Figure 1: Experimental set-up with SPLINTER

2.1 ORCA computer

The data acquisition system for the MAJORANA DEMONSTRATOR will be governed by a real time software able to control the run process and aid in the event build up. ORCA is a piece of software designed specifically for this type of experiments. ORCA is written in Objective-C [5] using the Cocoa [6] framework. Objective-C is the primary language used to write Apple's Mac software. The Cocoa frameworks consist of libraries, APIs, and runtimes that form the development layer for all of Mac OS X. The selection for the tools to code ORCA makes the application available only to Mac computers. This architecture makes using ORCA potentially more expensive, since it can only use Mac hardware rather than more generic hardware, but it makes the software very stable, since the compiler and libraries are maintained by Apple.

ORCA features a user friendly graphical user interface with all the necessary elements to build a DAQ. It is designed to aid the debugging of such systems, and implements powerful scripting capabilities to control and manipulate acquired data. The process of integrating new objects in ORCA is vital to keep the framework up to date. Appendix A presents a rough guide describing this process.

2.2 VME64 crate

The ORCA computer communicates with the VME crate via a SBC. The SBC acts as a middle man in the information exchange, polling the cards, extracting information via the VME bus and sending it back to the controller computer via Ethernet. In the experimental set-up a Concurrent Technologies VX 405/041[7] was used. The VX 405/041 is a single-board computer with embedded electronics to communicate with the VME bus architecture. It was designed as a powerful computer based upon the Intel Core Duo processor, Intel 945GM Express chipset with Graphics Controller, an 82573L single channel Gigabit Ethernet controller, an 82571EB dual channel Gigabit Ethernet controller and Universe II VME bus controller. This piece of hardware runs an embedded systems version of Linux. The card is capable of running the software that controls each VME card in the crate. There are several actions required to set-up the communication of the controller computer and the SBC. These actions are explained in the ORCA web reference [8]. Figure 1 show the experimental VME64 crate used at UNC. The Struck board features eight mini Lemo input connectors. The Gretina board uses a highly integrated cable connector. In Figure 2 the breakout cable for this high integrated connector is shown. This feature has been identified as a source of noise, since the breakout cable does frequently short the grounds among several input lines. This modifies the ground scheme and inserts a spike in the digitized signal.

Figure 2: From left to right, SBC, Struck 3302, Gretina 4 and dual channel HV supply in the experimental VME64 crate.

Table 1 presents the different features for both digitizer cards. One of the aspects worth noting is the trace transmitted trace length. It is clear that the longer the acquired trace the more information about the event that can be extracted. The amount information is crucial for the successful application of several cuts applied to the data to improve performance. Also worth noting in this table is the unusually wide input range of both cards. Although this feature might help with the energy range of the instrument, the frequency response of the front end of the digitizer can potentially damage the energy resolution of the experiment.

	SIS 3302	Gretina
# channels	8	10
Resolution (bits)	16	14
Sampling freq. (MSPS)	100	100
Firmware version	15.10	-
Input impedance (ohms)	50	50
Trace length (us)	2	8

Input range (Vpp)	5	6

Table 1: MAJORANA DEMONSTRATOR candidate digitizer boards features.

2.3 Faraday cage

One of the sources of noise in the experimental set-up was identified to be electromagnetic interference (or EMI, also called radio frequency interference or RF). This physical phenomena induces a disturbance in the electromagnetic field that affects an electrical circuit due to either electromagnetic induction or electromagnetic radiation emitted from an external source. These disturbances may interrupt, obstruct, or otherwise degrade or limit the effective performance of the digitizer board. The source may be any object, artificial or natural, that carries rapidly changing electrical currents (electronics crate, the oscilloscope, a cell phone, lights…). This phenomena was partially mitigated by transporting the experimental set-up inside a Faraday cage. Some of the sources of noise are part of the data acquisition system and were brought in to the cage as part of the experimental set-up, such as the VME crate. Figure 3 shows a oscilloscope screen capture, showing the induced signal in a 50 ohms coaxial wire connected to the oscilloscope. The 200kHz ripple is due to the oscilloscope's screen radiation. During this screen shot all equipment inside the Faraday cage was turned off. This is just an oscilloscope and a regular coaxial connected to it. Figure 4 shows the same oscilloscope screen capture after turning on the VME crate.

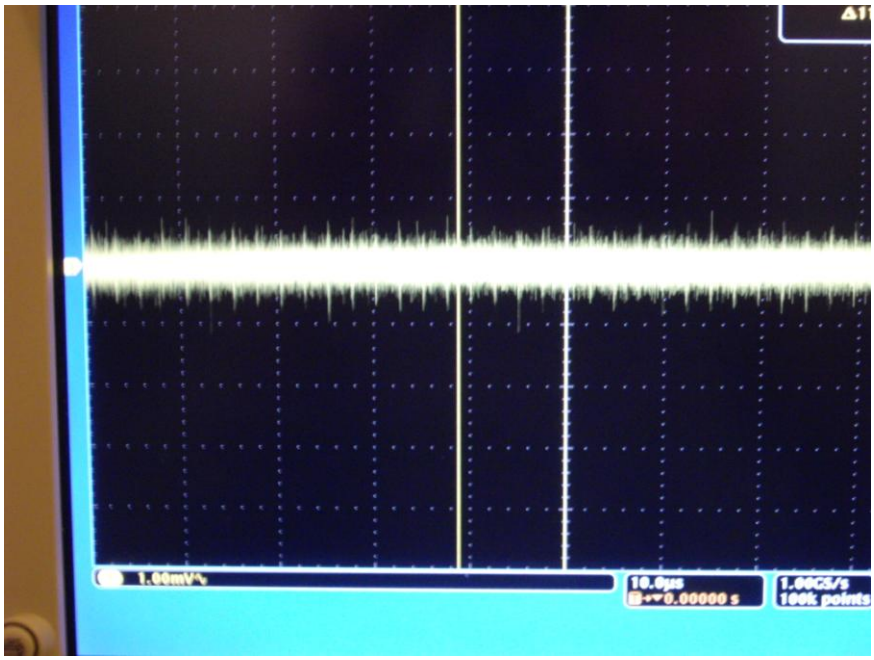

Figure 3: Base line inside the Faraday cage.

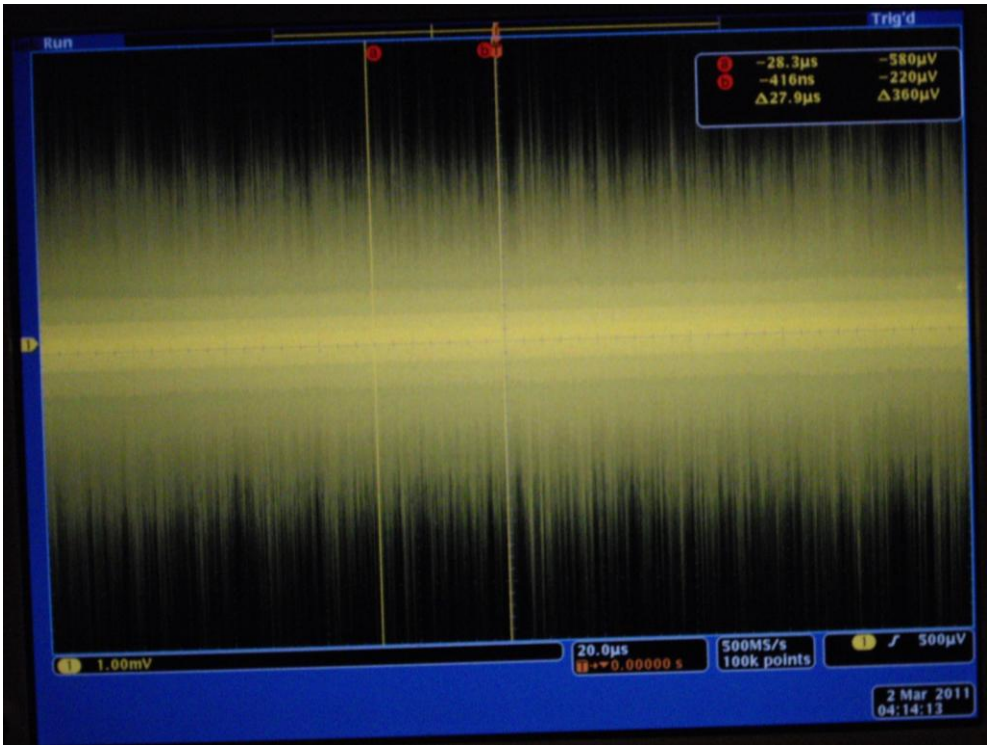

Figure 4: Base line of the experimental set-up with the VME64 crate on.

3 Digitizer experimental analysis

Using the set-up described in the previous section, a pulse generator (Agilent) was used to characterize the digitizer performance. These measurements were taken inside the Faraday cage and are intended to be guidance to minimum expected performance. The experimental measurement set-up was not optimized for the measurements; in particular the grounding of the experiment was not a star ground.

3.1 Effective Number of Bits

This measurement was done using the lowest amplitude setting in the pulse generator (10mV) and using a square waveform output. The signal to noise ratio derived in this section does not include a gain stage coming from the detector. Again, this should be interpreted as a reference value.

Figure 5 shows an acquired trace using the SIS3302. The trace shows a channel number difference slightly below 100 units. With an expected resolution of 76 uV/ch (5V/65536 channels) this is an expected result. The ripple of the base line swing a maximum of 64 channels approximately, this set the effective number of bits for the SIS 3302 card to 11 bits.

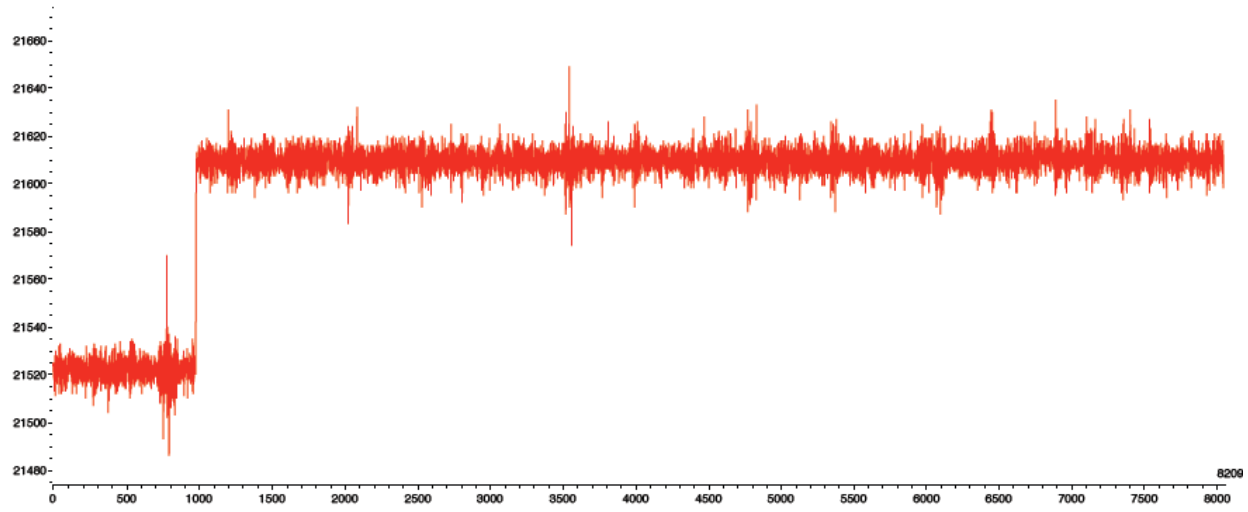

Figure 5: SIS 3302 10 mV square wave digitized. Graph shows channel number versus sample number.

Figure 6 shows an acquired trace using the Gretina. The trace shows a channel number difference slightly below 40 units. With an expected resolution of 0.35 mV/ch (6V/16384 channels) this is an expected result. The ripple of the base line swing a maximum of 16 channels approximately, this set the effective number of bits for the Gretina card to 10 bits.

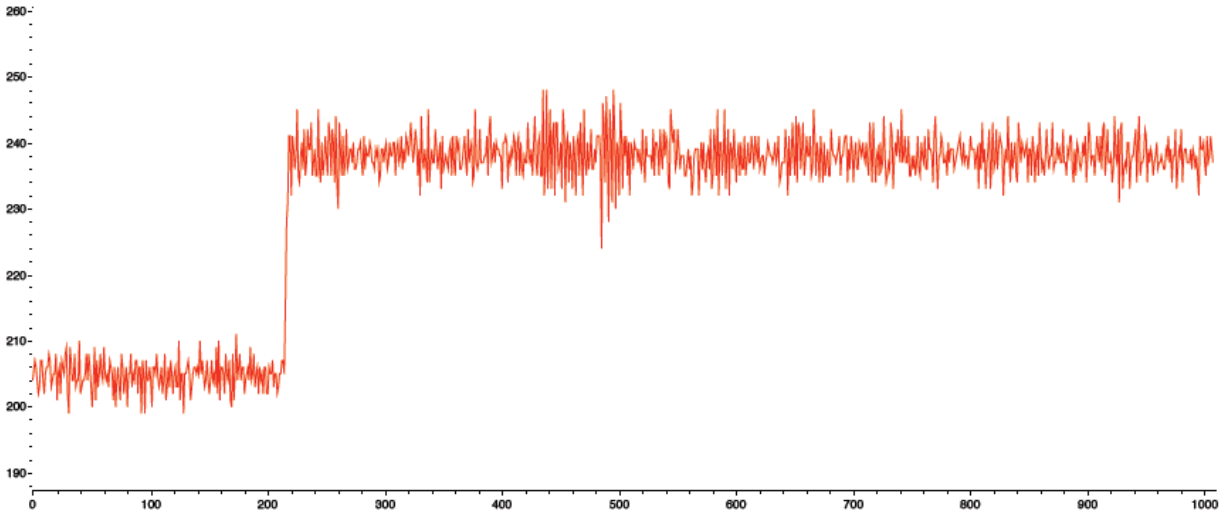

Figure 6: Gretina 10mV square wave digitized. Graph shows channel number versus sample number

3.2 Input range linearity

The integral non-linearity refers to the deviation of each individual code from a line drawn along the input range of the digitizer board. Figure 7 presents the experimental data acquired using an Agilent pulse generator. The experimental points were determined varying the amplitude of the output pulse of the generator. The frequency of the output was kept at a low rate, 10 kHz. The shape of the wave used was a square wave. The 3302 shows a slightly better performance, having an effective range without non-linearity effects, up to 1 V. From 1 V and on in the input range the non-linearity can reach up to 11 LSB. The Gretina board shows an input range without this effect up to 0.5 V. The integral non-linearity can reach up to 9 LSB.

The differential non-linearity represents the non-ideal behavior of the code transitions. Ideally your input range and the number of bits must be matched to ensure no missing codes. The resolution of the ADC in number of bits represents the number of codes that must be present at all operating ranges. The Gretina shows a differential non-linearity of 5 LSB at 2.5 V. The 3302 presents a 10 LSB differential non-linearity at 2 V.

A factor often overlooked when feeding a signal into a digitizer input is the non-ideal behavior of the front end circuitry of high speed A/D converters. This ADC front-end circuitry plays a pivotal role in the overall system performance, since it is in the border line between digital and analog signal domains. This circuitry is intended to match the usable input range of the digitizer and the input signal. In order to preserve the most information coming from the detector front end, the bandwidth of this input stage should be a wide as possible. There are several ways to receive a signal before the digitation stage in high-bandwidth applications. Using active components (amplifiers, comparators…) which attenuate the high frequency components of the input signal, or using passive components (transformers, baluns, capacitors…) which attenuate the low frequency component of the input signal. The results presented in this section for the 3302 and the Gretina, are the expected results for an active digitizer front-end in both cards.

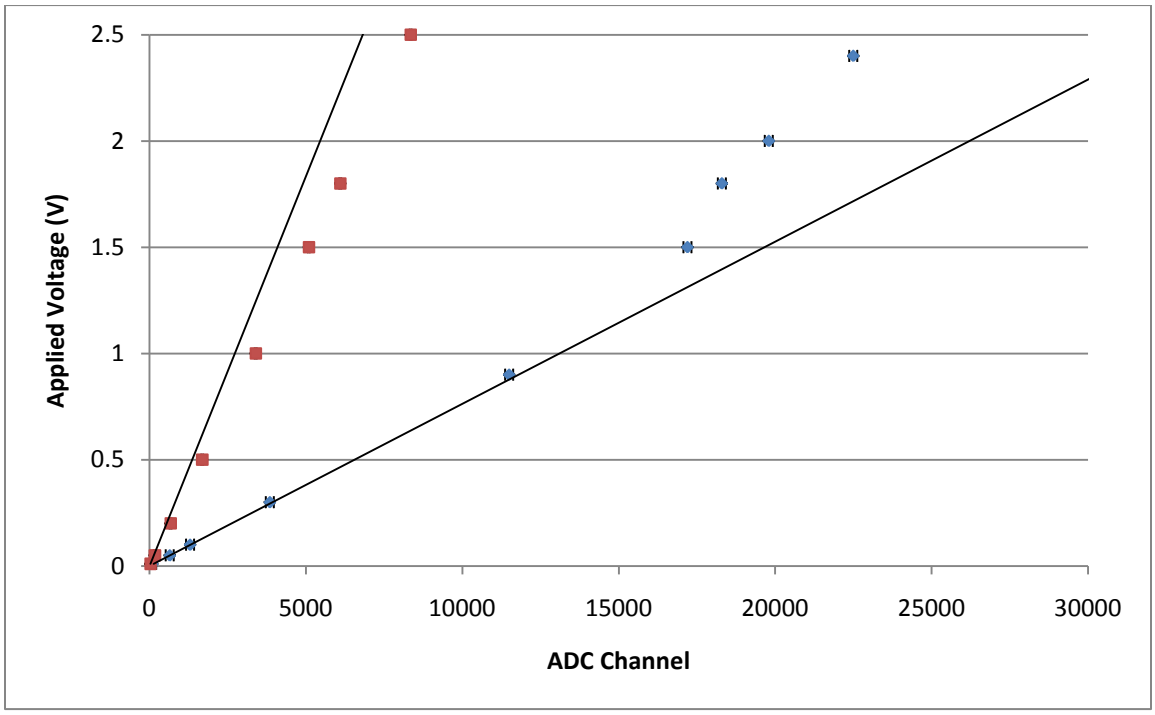

Figure 7: Applied voltage versus channel number for the Gretina4 (red squares) and the SIS3302 (blue diamonds) and their ideal linearity curves.

4 Digitizers on-board digital features

4.1 Gretina

The Gretina board receives the digital output of the ADC two Gaussian filters and computes the differential value of the actual sample against a user selectable delayed sample. Two 3-step Gaussian filters (14 bit and a 16 bit) are applied to the signal.

4.1.1 Trigger

The Gaussian filter output result is compared with a user selectable 15 bit value representing the unsigned LED threshold. The value at reset is 0x7FFF (full range so that no event should trigger). It is internally converted to a signed value depending on how the sign of the current sample is. The trigger module combines all the blocks needed to generate the LED timing. Figure 7 shows the information flow of this module.

4.1.2 Constant Fraction Discriminator

The board features circuitry that detects a zero crossing. This module raises a flag when crossing of a rising edge above a threshold or the crossing of a falling edge under a negative threshold.

4.1.3 Energy Filter

A hardware described trapezoidal filter with the extremum search has been implemented in the reprogrammable logic device in order to create an energy value. It simply implements the following equation:

$$Y_n = Y_{n-1} + ((X_n + X_{n-2m-k}) - (X_{n-m} + X_{n-m-k}))$$

Where n is the sample number, k is the sample delay and m is the digital filter. It is worth noting that the filter output is given in 2's complement representation.

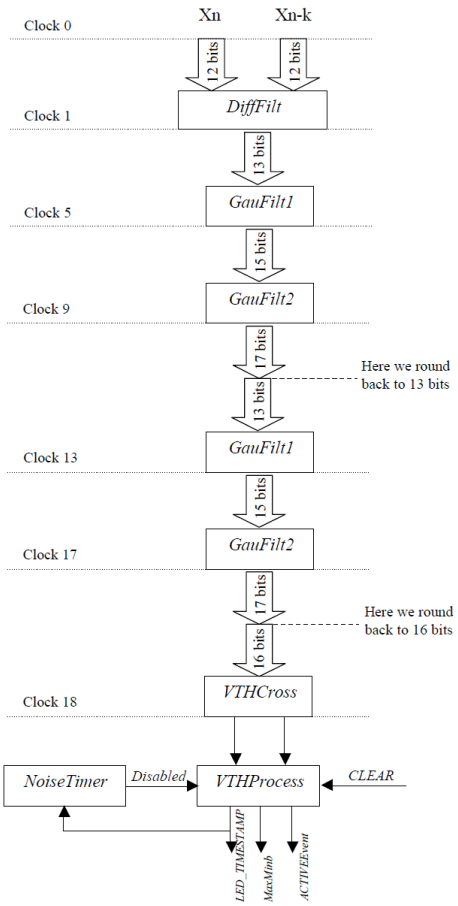

Figure 8: Gretina Digitizer Board Leading Edge Discriminator (LED) Flow Chart. From [9]

4.2 SIS3302

4.2.1 Trigger

A trapezoidal FIR filter is implemented for each ADC Channel to generate a trigger signal. This trigger signal can be used to trigger the sample logic immediately or it can be routed to SIS3302 Lemo output connector. The trigger circuitry features:

- Programmable decimation (1 / 2 / 4 / 8 / 16 Clocks)
- Programmable Peaking Time (max. 511 Clocks)
- Programmable SumGap Time (max. 511 Clocks)
- Programmable Trigger pulse out length (max. 255 Clocks)
- Programmable Trigger Threshold

4.2.2 Energy filter

A trapezoidal FIR filter is implemented for each ADC Channel to generate a "moving window average" stream (MWA). A decimation logic (average, integration) is also implemented. The energy filter circuitry features:

- Programmable decimation (1 / 2 / 4 / 8 Clocks)
- Programmable Peaking Time (max. 1023 Clocks)
- Programmable Gap Time (max. 255 Clocks)

Energy Tau correction factor is implemented on board in this card. This feature is not documented. Probably it is an implementation of the ballistic deficit correction in a digital filter.

4.2.3 Timing information

The Struck card features a 48-bit Timestamp generator. This means that the whole DAQ can be synchronized without extra circuitry, just routing the same clock and reset to all cards.

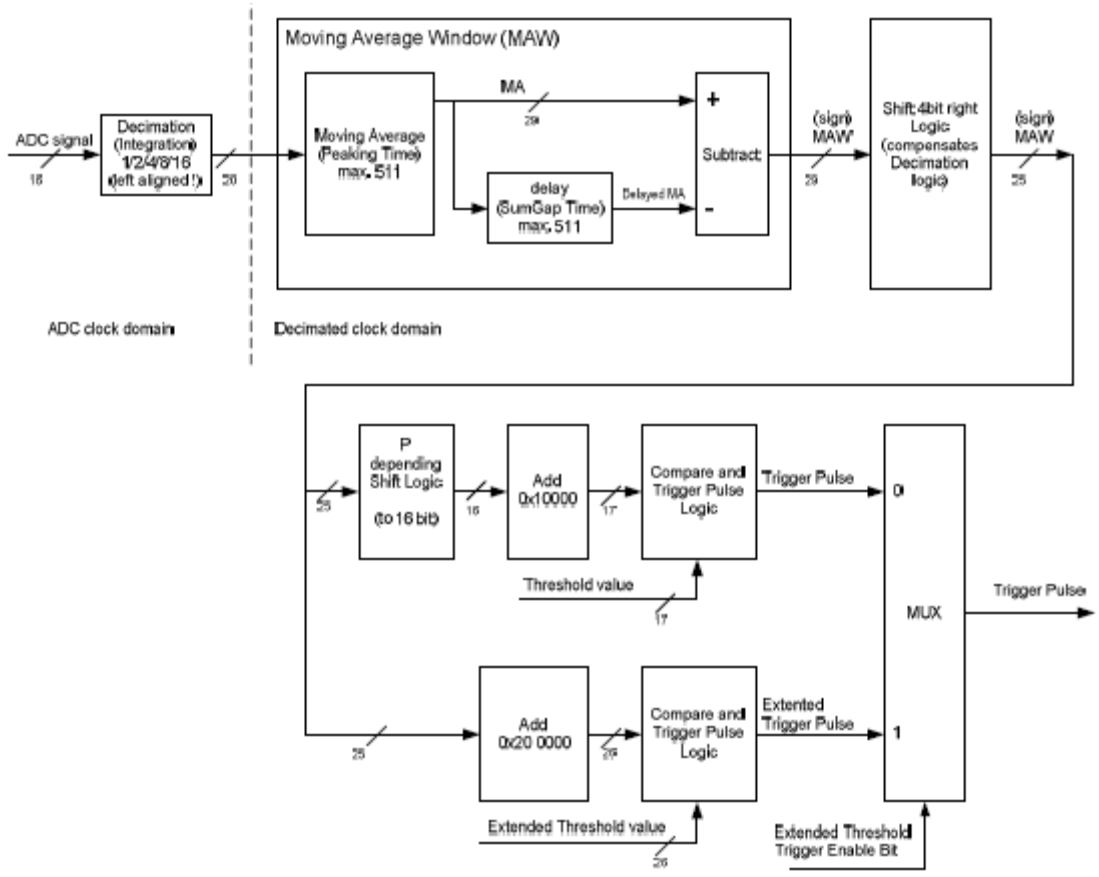

Figure 9: Block diagram of the trigger unit implemented in the 3302

5 Digitizer control using ORCA

The ORCA framework will be used along with the cards to build the backbone of the MJD DAQ. The two objects behave slightly different, mainly due to the different architectures of the boards. This section explains the operability of the objects for each card.

5.1 Gretina ORCA Object

The Gretina object is very intuitive to use thanks to its layout, although the actual shipping of the data is not present in the object. Pile-up controls are present in the object controllers, but it should be an option to ship its content or not. The LED threshold value is a 13 bit register; the threshold by default in this object has the value after reset 9in other words don't set the value of this register above 16383 and this is a complements 2 number, so LED trigger at O V corresponds to a value of 8191). The enable for each channels are showed in the left most column of controllers. There is a debug mode for the channels. It is not clear how the MJD could use this feature. The card communicates with this object seamlessly and a probe board button is useful to make sure the board is not hanging and is being polled correctly. Figure 9 shows the ORCA object GUI for the Gretina card. The configuration shown is used during the experimentation presented in this document.

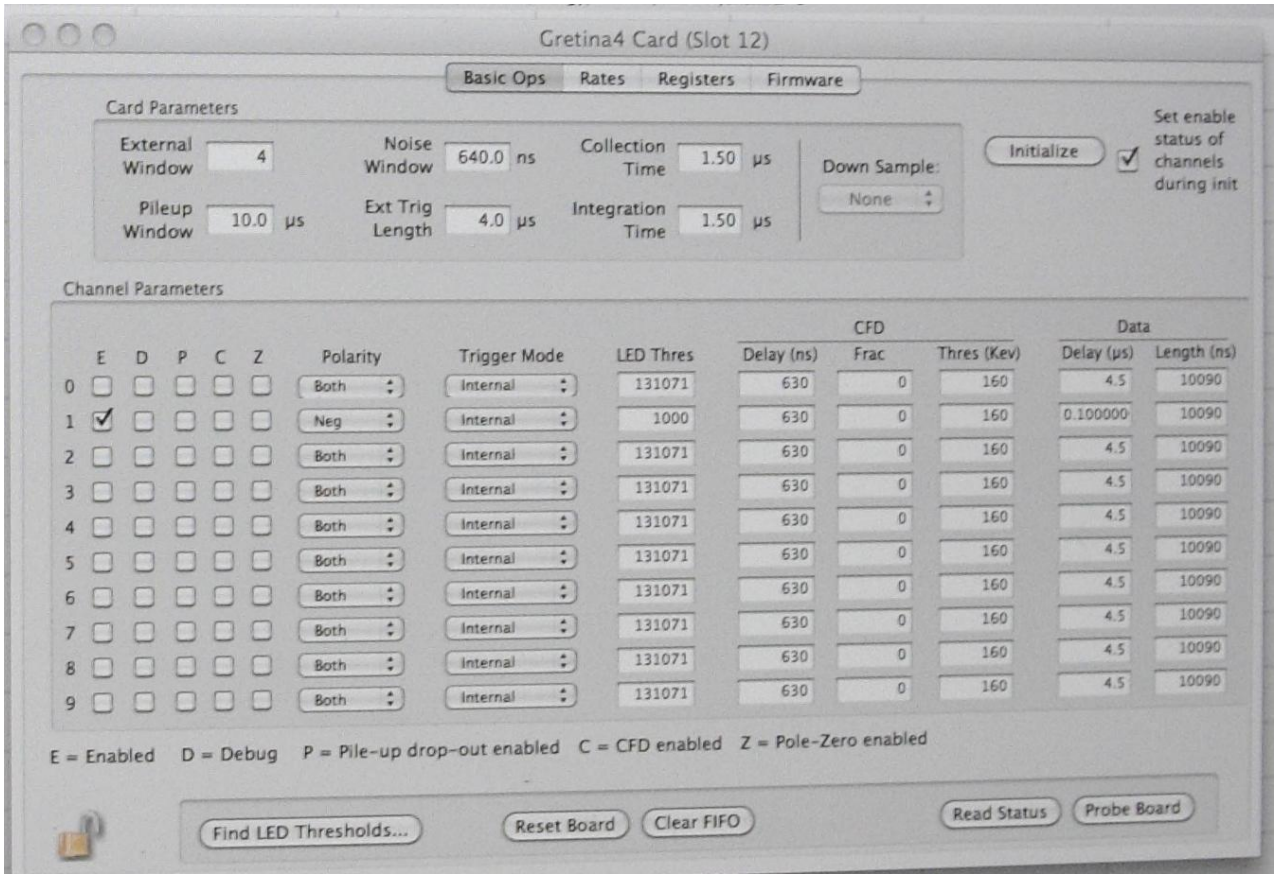

Figure 10: Gretina ORCA object screen capture.

5.2 SIS 3302 ORCA Object

The SIS3302 object represents the flexibility of the board is an orderly way. The first issue that an operator might encounter is that the board address default value is not a 32 bit value, and the board address does not refer to the position of the board in the rack, is the hardware board address of the board. The clock selected by default by the object is a buggy clock source, so one should immediately change to another clock source. The other issue in the control is that one cannot just one of two the gate checkmarks (int and ext) checked, the board would then wait for a gate to trigger. The DAC offset, is the offset injected by the board to the input signal, not a trigger offset. Lemo connector options might not be required for the MJD DAQ set-up.

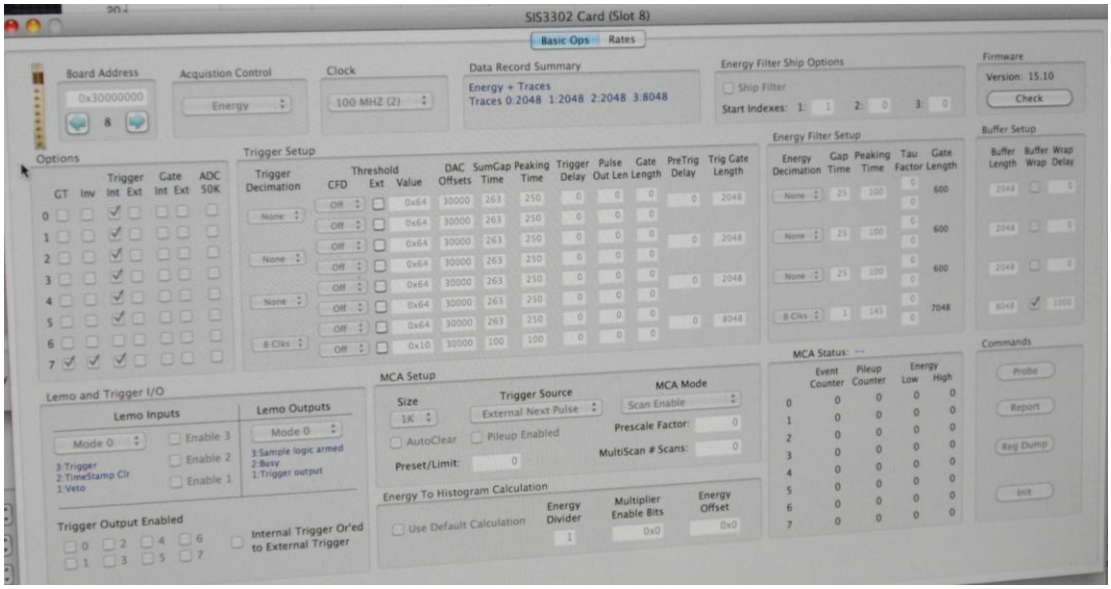

Figure 11: SIS3302 ORCA object screen capture.

6 Digitizer Evaluation

6.1 SIS3302 issues

- Wide input range: The card exhibits a very wide input range, and it takes a toll in its linearity performance. For this card a custom front-end must be requested from the vendor, with a narrower input range and an input signal bandwidth matched to the detector signal.
- Gated trigger: When operating the 3302 it is noticeable the use of a gate in the trigger stage. This feature could be useful in detector arrays that trigger each other. For example the veto panels could inhibit the read out cards. This is not the modus operandi envisioned for the MJD. A time stamp will be generated for every recorded event, and matched in an offline analysis with veto events using GAT. This feature should be removed from the card.
- Input wiring: The card takes 8 mini Lemo cables. This is not ideal, since the cost and grounding schemes get more complicated with this type of input connectors when dealing with a large number of channels.
- Documentation: Although not as bad as the Gretina, the documentation for the 3302 lacks of a good description of the input front stage, but it is sufficient to understand the architecture.
- Dead time: This is the trade-off of having a long buffer size. Dead time when using 8K is 88 us. This value could affect the acquisition efficiency of the neutrino less signal.
- Poor low frequency response of the input stage. This is usually inherited from the use of a decoupling capacitor on the inputs. Figure 12 shows the damaging effects in signal wave form.

6.2 Gretina issues

- Wide input range: The card exhibits a very wide input range, and it takes a toll in its linearity performance. For this card a custom front-end must be requested from the vendor, with a narrower input range and an input signal bandwidth matched to the detector signal.
- Limited trace buffer: This is the trade-off of having a short buffer size.
- Noisy Breakout input connector: It was an issue for the experimental set-up described in this document, to have the grounds touching each other freely. The highly integrated connector could help simplify the wiring of the DAQ system and potentially could shield the lines with just one electromagnetic shield shared by all lines, instead of having every line have it own shield.
- Complex on-board filtering: Several Gauss filter and a differential approach of the sample analysis, makes understanding the card hard, and it is obviously designed like that for a specific purpose, not the MJD one though.
- Energy filter simplicity: All the features of the card are very complex, but the trapezoidal filter for the energy value. It is a circuitry optimized for execution speed, not for optimal resolution.

- Documentation: The Gretina documentation is encrypted in semi-VHDL language, and the features of the card are barely documented.
- Poor low frequency response of the input stage. This is usually inherited from the use of a decoupling capacitor on the inputs. Figure 12 shows the damaging effects in signal wave form.

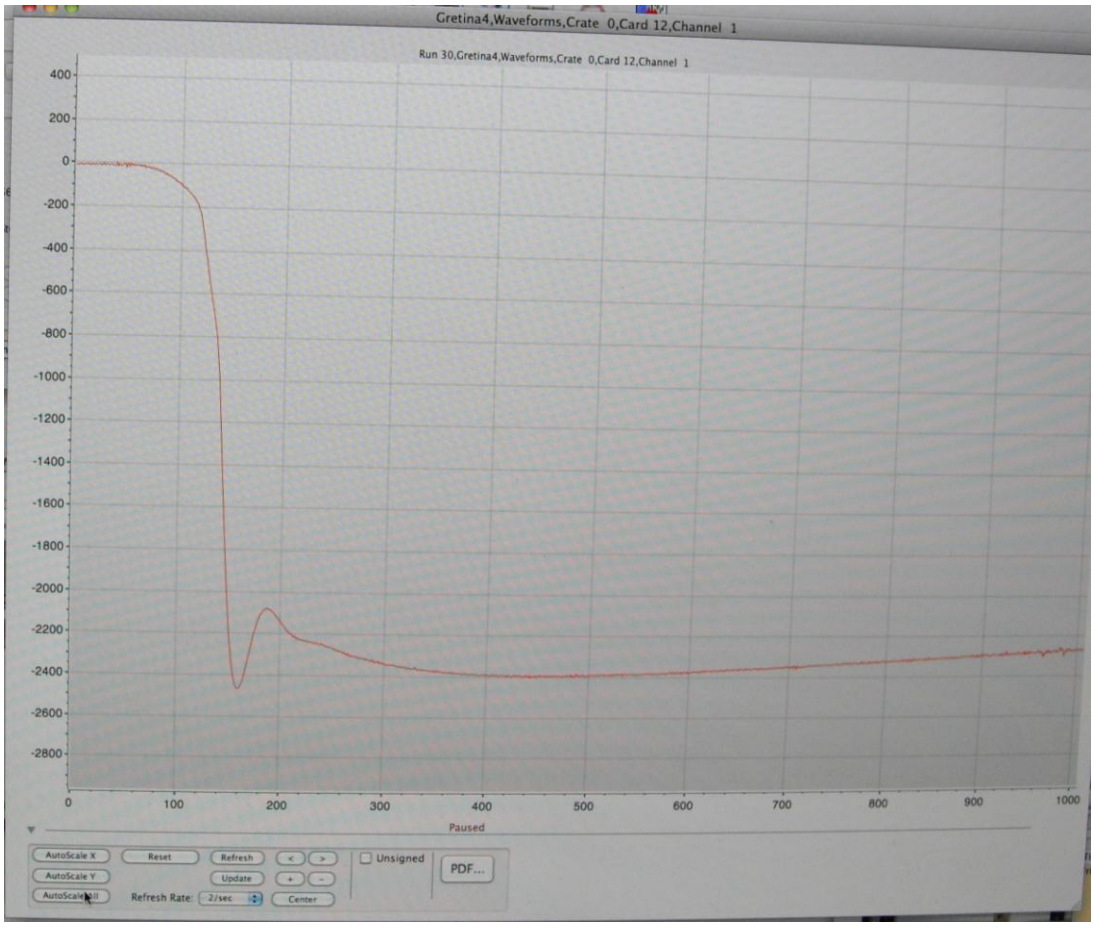

Figure 12: Raw waveform capture from a Gretina acquired event using SPLINTER

7 Recommendations

The information contained in this document is not the full characterization of a detector channel, which could give a better idea of the optimal digitizer board by testing all elements together. That way the gain stage could be optimized and the input range and bandwidth determined accurately. With the experimental set-up described in this document, the recommendation issued by the author is to use the Struck 3302 card. Its configurable trapezoidal filtering for trigger and time stamp generation are features that the MJD will use, and the card can be tuned to ensure optimal performance in terms of data transmission and on-board filtering. The input connector scheme should be reworked on the card, so the wiring can be shielded with a single ground plane and the ground of the analog stage in the card should be routed through the front panel of the card so it can be optimally configured in the star ground scheme.

8 References

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